Asian Journal of Applied Science and Technology (AJAST)
Volume 1, Issue 1, Pages 195-198, February 2017

Distortion Correction Scheme for Multiresolution Camera Images

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Article Received: 17 February 2017 *Article Accepted: 27 February 2017* *Article Published: 28 February 2017*

ABSTRACT

An efficient VLSI architecture implementation for barrel distortion correction in surveillance camera images is presented. The distortion correction model is based on least squares estimation method. To reduce the computing complexity, an odd-order polynomial to approximate the back-mapping expansion polynomial is used. By algebraic transformation, the approximated polynomial becomes a monomial form which can be solved by Horner's algorithm. The proposed VLSI architecture can achieve frequency 218MHz with 1490 logic elements by using 0.18µm technology. Compared with previous techniques, the circuit reduces the hardware cost and the requirement of memory usage.

Keywords: Barrel distortion correction, Least squares estimation, Surveillance and Horner's algorithm.

1. INTRODUCTION

Nowadays, surveillance camera is commonly used in public and private places such as government buildings, military bases, car parks, and banks, and so forth. Surveillance camera can capture the entire region of interest with cameras as few as possible if cameras with large field of view are adopted. Surveillance cameras are video cameras used for the purpose of observing an area. It is connected to a recording device or IP network, and may be watched by a guard. Cameras and recording equipment used to be relatively expensive and required human personnel to monitor camera footage, but analysis of footage has been made easier by automated software that organizes digital video footage into a searchable database, and by video analysis software. The amount of footage is also drastically reduced by motion sensors which only record when motion is detected. With cheaper production techniques, surveillance cameras are simple and inexpensive enough to be used in home security systems, and for everyday surveillance.

The distortion correction circuit may be included in end-user camera equipment's, so how to implement it with lower hardware cost is an important issue. To reduce more hardware, algebraic transformation is used to replace all the vector magnitude square by a new variable. It makes the new combined polynomial becomes a monomial form. Therefore, Horner's algorithm [6] is able to efficiently evaluate the results of back-mapping and polar to Cartesian coordinate transformation. This approach not only greatly decreases the calculation complexity of back mapping but also provides a flexible architecture for different designs by time multiplexed technique [7], [8]. To reduce more hardware costs and power consumption, we also implemented a low cost linear interpolation circuit by algebraic manipulation technique. It greatly eliminates the number of multipliers from eight to three. In this paper, a low- cost, low-power, and low memory requirement distortion correction circuit is designed for surveillance or wide-angle camera applications.

2. OVERVIEW OF DISTORTION CORRECTION TECHNIQUE

In this section, least-square estimation method is used for distortion correction technique. Barrel distortion can be corrected by two main tasks: 1) back mapping of all pixels in CIS onto DIS, and 2) calculating the intensity of every pixel in CIS by linear interpolation [7]. The block diagram of the distortion correction procedure is shown in Fig1. First the transformation mapping from rectangular coordinate to polar coordinate for all pixels is done. Then, a back mapping procedure is introduced to decrease the computing complexity and polar to rectangular coordinate steps by eliminating the angle θ and reducing the square root operation for ρ. Finally, a basic algebraic manipulation is used to decrease the arithmetic resource of the linear interpolation.

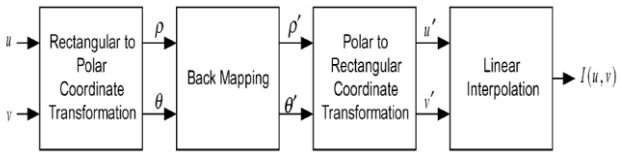

Fig.1. Block diagram for distortion correction procedure

The first step of the proposed distortion correction technique is transforming all pixels in the distorted image space (DIS) onto the corrected image space (CIS) i, e., this step is to convert rectangular to polar coordinate. The distortion center is (u'_c, v'_c) in DIS and the correction center is (u_c, v_c) in CIS. In DIS, (u', v') is the Cartesian coordinate and (ρ', θ') is the polar coordinate. The distance ρ' from distortion center (u'_c, v'c) to an image pixel (u', v') and the angle θ' between the pixel and distortion center are given by

$$\rho' = \sqrt{(u' - u'_c)^2 + (v' - v'_c)^2} \quad (1)$$

$$\theta' = arc\tan\left(\frac{v' - v'_c}{u' - u'_c}\right) \quad (2)$$

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The distance ρ from distortion center (u_c ,v_c) to an image pixel (u, v) and the angle θ between the pixel and distortion center are given by,

$$\rho = \sqrt{(u-u_c)^2 + (v-v_c)^2} \quad (3)$$

$$\theta = \arctan\left(\frac{v-v_c}{u-u_c}\right) \quad (4)$$

The second step is back-mapping process which will map the pixel (ρ, θ) in CIS to (ρ', θ') in DIS. The back mapping procedure can be defined by a back mapping expansion polynomial of degree N as,

$$\rho' = \sum_{n-1}^{N} b_n p^n \quad (5)$$

$$\theta' = \theta \quad (6)$$

Where b_n is the back mapping coefficient which can be obtained by the least-squares estimation method.

The third step is to perform the polar to rectangular coordinate conversion. The location (u', v') in DIS can be calculated as,

$$\begin{aligned} u' &= u'_c + \rho' cos\theta' \\ v' &= v'_c + \rho' sin\theta' \end{aligned} \quad (7)$$

The next step is to perform linear interpolation. Here, the pixel (u', v') location need not be an integer location. Its intensity value can be calculated by linearly interpolating with the intensity values of the four neighboring pixels (u', v') around in DIS.

2.1 Simplified Back-Mapping Procedure

As mentioned above, the odd order polynomial is high-approximation to the back mapping expansion polynomial is used. The back mapping expansion polynomial can be approximated to odd-order polynomial as,

$$\rho' = c_0\rho + c_1\rho^3 + c_2\rho^5 + c_3\rho^7 + \cdots \quad (8)$$

Where *c*0, *c*1 , *c*2 , *c*3 . . . are back-mapping coefficients of the odd-order back-mapping polynomial.

There are two steps to reduce the computing resources of back-mapping procedure. The first is eliminating the calculation of θ. According to (7), the *θ* and θ' are the same. Thus, the cos *θ* and sin *θ* can be obtained as,

$$\sin\theta = \sin\theta = \frac{v-v_c}{\rho} \quad (9)$$

$$\cos\theta = \cos\theta = \frac{u-u_c}{\rho} \quad (10)$$

In below equations mentioned, here no odd power of ρ exists, so the square-root calculation for ρ can be removed.

$$u' = u'_c + \rho' \cdot \frac{u-u_c}{\rho}$$

$$u' = u'_c + (c_0 + c_1\rho^2 + c_2\rho^4 + c_3\rho^6 \ldots\ldots)' \cdot (u-u_c)' \quad (11)$$

$$v' = v'_c + \rho' \cdot \frac{v-v_c}{\rho}$$

$$v' = v'_c + (c_0 + c_1\rho^2 + c_2\rho^4 + c_3\rho^6 \ldots\ldots)' \cdot (v-v_c)' \quad (12)$$

Thus, the complex square-root calculation is eliminated because both u' and v' are calculated with ρ^2 rather than with ρ.

3. HORNER'S ALGORITHM

The main purpose of Horner's algorithm [16] is to efficiently evaluate the polynomials in monomial form.

Given the polynomial,

$$\begin{aligned} p(x) &= \sum_{i=0}^{n} a_i x^i \\ p(x) &= a_0 + a_1 x + a_2 x^2 + \ldots\ldots + a_n x^n \end{aligned} \quad (13)$$

Where a_o, $a_{1,\ldots,}a_n$ real numbers, then to evaluate the polynomial at a specific value of x, say x_o. A new sequence of constants is defined as follows,

$$\begin{aligned} b_n &:= a_n \\ b_{n-1} &:= a_{n-1} + b_n x_0 \\ &\vdots \\ b_0 &:= a_0 + b_1 x \end{aligned} \quad (14)$$

Then b_o is the value of $p(x_o)$. Then the polynomial can be written as,

$$p(x) = a_0 + x\left(a_1 + x\left(a_2 + \cdots + x\left(a_{n-1} + a_n x\right)\cdots\right)\right). \quad (15)$$

Thus, by iteratively substituting the b_i into the expression,

$$\begin{aligned} p(x_0) &= a_0 + x_0(a_1 + x_0(a_2 + \cdots + x_0(a_{n-1} + b_n x_0)\cdots)) \\ &= a_0 + x_0(a_1 + x_0(a_2 + \cdots + x_0(b_{n-1})\cdots)) \\ &\vdots \\ &= a_0 + x_0(b_1) \\ &= b_0. \end{aligned} \quad (16)$$

As described above, an iteration function is used to rewrite the polynomial. The function p^n which is the *n*th iteration of p can be represented as $p.p^{n-1}$ and it is defined as

$$p^n = p.\ p^{n-1} \quad (17)$$

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To rewrite the polynomial as iteration function, the evaluated polynomial at the specified value of $x = x_o$ can be represented as,

$$p(x_o) = (c_{n-1}+c_n.x_o.p^{n-1}(x_o) \quad (18)$$

The polynomial is evaluated to compute $p(x_o)$ where x_o is a constant.

The Horner's algorithm is executed by following the below steps:

Step 1. Set $u = n$ (where n is the degree of the polynomial)
Step 2. Set Result = Cn.
Step 3. If $u = 0$ stop. Answer is Result.
Step 4. Compute Result =Result × xo + Cu−1.
Step 5. $u = u - 1$.
Step 6. Go to step 3.

By Horner's algorithm, the computing complexity of the evaluating polynomial can be decreased. The complexity of back mapping and polar to rectangular coordinate steps can be reduced in the same way.

4. PROPOSED VLSI ARCHITECTURE

Fig.2. shows the block diagram of proposed architecture. In this design, when the start signal is enabled, the circuit will output the intensity value of the first pixel after 21 clock cycles. Then, it can process one pixel in CIS per clock cycle. Totally, it would take (1024 x 728 + 21) cycles to process an image with 1024 x 728 pixels. This design consists of four main modules: mapping unit, memory bank, linear interpolation unit and controller. The memory bank is composed of solid state drives and RAM. The interpolation unit linearly interpolates the final intensity value. The controller provides the control signals of each state to other units and handles the whole correction procedure. The detailed circuits of mapping and linear interpolation units are described as follows.

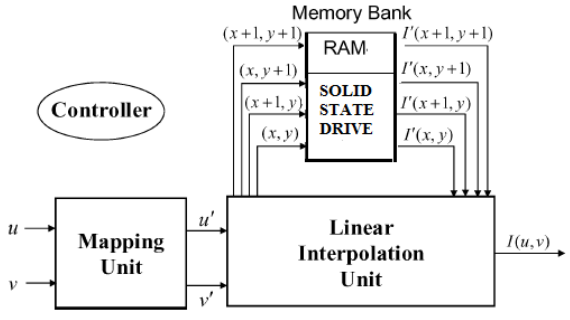

Fig.2. Proposed VLSI Architecture

For each pixel (u, v) in CIS, the mapping unit performs the operations needed to calculate (u', v'). Most multipliers and adders are realized with 24-bit width as adopted in [6]. According to the simulation results obtained from XILINX, it was found that the propagation delay of a 24-bit multiplier is quite long. Hence, the 15-bit two-stage pipelined multiplier is adopted in the design to get better pipeline scheduling. Fig 3. shows the 15-stage pipelined architecture of the mapping unit. The linear interpolation unit obtains the intensity values of the four neighboring pixels around (u', v') and calculates the final intensity value I (u, v). Fig.4. shows the 6-stage pipelined architecture of the linear interpolation unit which performs the operations needed to calculate I (u,v).

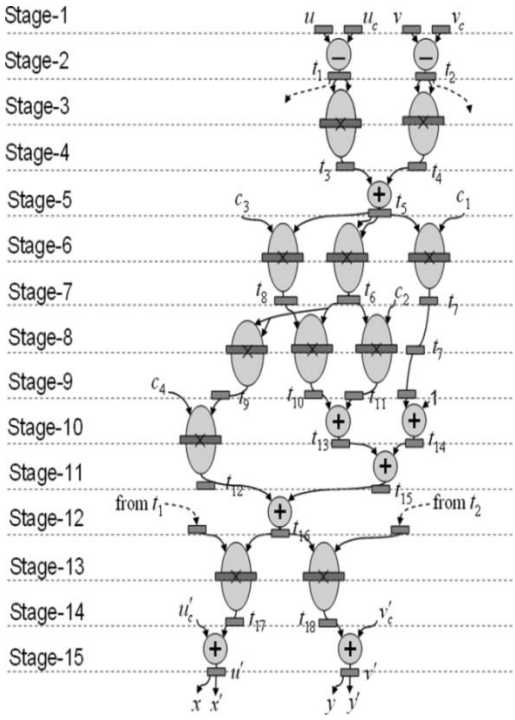

Fig.3. 15-stage pipelined architecture of mapping unit

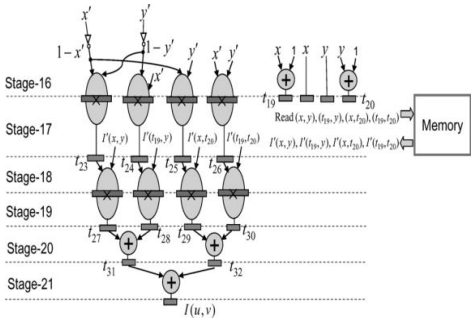

Fig.4. 6-stage pipelined architecture of linear interpolation unit

5. RESULTS AND DISCUSSION

The VLSI architecture of the proposed design was implemented by using Verilog HDL. Here MATLAB is used to convert the image file to grey scale image. Table 1 shows the Simulation Results of two designs using Altera EP20K600EBC652-1X FPGA the size the design with TSMC's 0.18 m cell library. The results show that the design contains 1490 logic elements. It works with a clock period of 5 ns and operates at a clock rate of 218 MHz.

Table 1. Comparative Analysis

Paper	Logic Elements	Clock rate	Throughput
[13]	1686	200MHz	14Mpixels/s
Proposed	1320	210MHz	21Mpixels/s

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6. CONCLUSION

In this paper, a low-cost, low-power, and low memory requirement VLSI architecture of distortion correcting circuit was presented for surveillance images. The computing complexity of correcting functions is reduced by Horner's algorithm and the algebraic manipulation of the linear interpolation. This provides an efficient and effective approach to eliminate the distortion. It provides a logic element of about 1490, clock rate of 218MHz and throughput of 21Mpixels/s. From this it is proved that this algorithm has high performance than other existing VLSI correcting designs.

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