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Performance Analysis of Dual Gate MOSFET in Adder

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ABSTRACT

This paper describes a parallel single-rail self-timed adder using dual gate MOSFETs which is based on a recursive formulation for performing multi bit binary addition. Thus the addition is parallel for those bits that do not need any carry chain propagation and the circuit attains logarithmic performance over random operand conditions without any special speedup circuitry or look-ahead schema. A practical design of dual gate MOSFET is provided along with a completion detection unit. The design is regular and does not have any practical limitations of high fan outs. A high fan-in gate is required on the design but this is unavoidable for asynchronous logic and is managed by connecting the transistors in parallel. Simulations have been performed using LT spice tool that verify the practicality and superiority of the proposed approach over existing asynchronous adders.

Keywords: Asynchronous circuits, DGMOSFET design, Binary adders and Digital arithmetic.

1. INTRODUCTION

Binary addition is one of the most important operations that a processor performs. Most of the adders have been designed using synchronous circuits even though there is a strong interest in clock less/ asynchronous processors/circuits. Asynchronous circuits are those which do not assume any quantization of time. Therefore, they hold a great potential for logic design as they are free from several problems from clocked (synchronous) circuits. In general, logic flow in asynchronous circuits is controlled by a request acknowledgment handshaking Protocol signals to establish a pipeline in the absence of clocks.

Explicit handshaking blocks are small elements, such as bit adders, are expensive. Therefore, it is implicitly and successfully managed using dual-rail carry propagation in adders. A valid dual-rail carry output also provides an acknowledgment signal from a single-bit adder block. Thus, asynchronous adders are based on either full dual-rail encoding of all signals (more formally using null convention logic that uses symbolically correct logic instead of Boolean logic) or pipelined operation using single-rail data encoding and dual-rail carry representation for acknowledgment signals. While these constructs add robustness to circuit designs and they also introduce significant overhead to the average case performance on asynchronous adders add benefits.

Therefore efficient alternative approach that can address these problem presents an asynchronous parallel self-timed adder (PASTA) using the algorithm originally proposed. The design of PASTA using dual gate MOSFET is regular and uses half-adders (HAs) along with multiplexers requiring minimal interconnections. Thus, it is suitable for implementation VLSI circuits. The design works in a parallel manner which is unique as it employs feedback through XOR logic gates to constitute a single-rail cyclic asynchronous sequential adder. Cyclic circuits can be more efficient on resource than their acyclic counterparts. On the other hand, wave pipelining (or maximal rate pipelining) is a technique that can apply pipelined inputs before the stabilization of outputs. The proposed circuit manages automatic single-rail pipelining of the carry inputs which is separated by propagation and inertial delays of the gates in the circuit path. Thus a single rail wave-pipelined approach is effective and quite different from conventional pipelined adders using dual-rail encoding to implicitly represent the pipelining of carry signals independent carry chain blocks.

2. PARALLEL ADDERS

Parallel adders are combinatorial circuit which is not clocked, does not have any memory and feedback circuit elements for adding every bit position of the operands in the same time. Fig 1 shows the parallel adder thus it requiring number of bit-adders which consists of (full adders + 1 half adder) equal to the number of bits to be added.

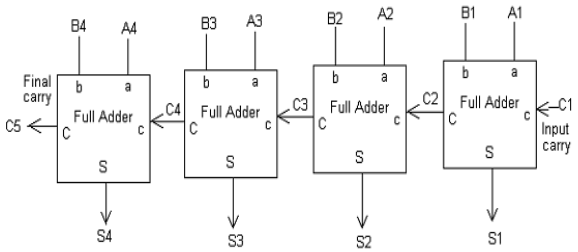

Fig.1. Parallel adders

3. SELF TIMED CIRCUITS

An asynchronous circuits are also called self-timed circuit, is a sequential digital logic circuit which is not governed by a clock circuit or global clock signal. Instead they always use signals that show completion of instructions and operations, specified by simple data transfer protocols. This type is varied from synchronous circuit in which changes to the signal values in the circuit are triggered by repetitive pulses called a clock signal. However asynchronous circuits have the

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potential to be faster, and may also have other advantages in lower power consumption, lower electromagnetic interference, and better modularity in large a system which has active area of research in digital logic design. In asynchronous circuits, there is absence of clock and the state of the circuit changes as soon as the input changes. Since they don't have to wait for a clock pulse to begin process of the inputs, asynchronous circuits can be faster than synchronous circuits, and their speed is theoretically limited only by the propagation delays of the logic gates. In principle, the asynchronous systems promise more advantages over synchronous systems: (i) lower power, since an asynchronous component computes only when necessary; (ii) higher performance, since global clock distribution and synchronization can be avoided and finally, (iii) greater modularity and ease of design, since there are no global timing constraints in the design.

There are myriad designs of binary adders and here on asynchronous self-timed adders. Self-timed defines a logic circuits that depend on and/or engineer timing assumptions for the correct operation. Self-timed adders have the ability to run faster averaged for dynamic data, as early completion sensing can avoid the need for the worst case bundled delay mechanism of synchronous circuits.

3.1 Pipelined Adders Using Single-Rail Data Encoding

The asynchronous Req/Ack handshake can be used to enable the adder block as well as to create the flow of carry signals over the circuit. In most of the cases, a dual-rail carry convention is obtained for internal bitwise flow of carry outputs. These dual-rail signals can represent more than two logic values (invalid, 0, 1), and that can be used to provide bit-level acknowledgment when a bit operation is completed. Final completion is sensed using all bit Ack signals are received at high. The carry-completion sensing adder is an example of a pipelined adder, which uses full adder (FA) functional blocks adapted for dual-rail carry. On the other hand, a speculative completion adder circuit is designed. It also called terminate logic and early completion to select the exact completion response from a number of fixed delay lines. However, the terminate logic implementation is expensive due to the necessary of high fan-in requirements.

3.2 Delay Insensitive Adders Using Dual-Rail Encoding

Delay insensitive (DI) adders are also asynchronous adders that declare bundling constraints or DI operations. Therefore, they can suitably operate in the presence of bounded but unknown gate and wire delays. There are many different DI adders, such as DI ripple carry adder (DIRCA) and DI carry look-ahead adder (DICLA). DI adders use dual-rail encoding and are expected to increase complexity. Though a dual-rail encoding doubles the wire complexity, they can still be used to produce circuits nearly as effective as that of the single-rail variants using dynamic logic or nMOS only designs. An example 40 transistors per bit DIRCA adder is designed in while the conventional CMOS RCA uses 28 transistors. Similar to CLA, the DICLA has carry propagate, generate, and kill equations in terms of dual-rail encoding. They do not connect the carry signals in a chain but organize them in a categorized tree. Thus, they can actually operate faster when there is long carry chain. Fig 2 shows the general block diagram of PASTA.

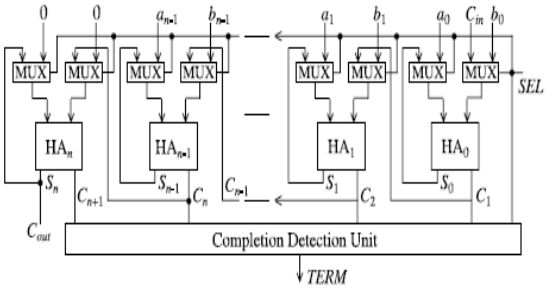

Fig.2. General block diagram of PASTA

A further optimization is obtained from the performance that dual rail encoding logic can benefit from settling of either the 0 or 1 path. Dual-rail logic need not wait for two paths to be evaluated. Thus, it is possible to additional speed up the carry look-ahead circuitry to send the carry-generate/carry-kill signals to any level in the tree. This is elaborated and referred as DICLA with speedup circuitry (DICLASP).

4. EXISTING SYSTEM

Fig.3 shows the adder first accepts two input operands to perform half additions for each bit. Subsequently it iterate on using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level and complete the process.

4.1 Parallel Self Timed Adder

The selection of input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and also switch to feedback/carry paths for subsequent iterations using SEL = 1. The feedback path from the half adders enables the multiple iterations to continue until the completion when all carry signals will assume zero values.

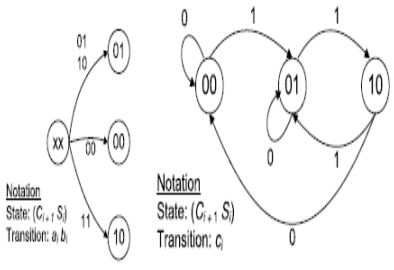

Fig.3. State diagrams for PASTA a) Initial Phase b) Iteration phase

4.2 State Diagram

Each state is represented by a (C_{i+1} S_i) pair where C_{i+1} S_i represent carry out and sum values respectively from the i_{th} bit adder block. Fig 3 shows the two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. During the initial phase the circuit simply works as a combinational HA operating in fundamental mode. It is

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apparent that due to the use of half adders instead of full adders state (11) cannot appear. During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated using SEL. The carry transitions (C_i) are allowable as many times as needed to complete the recursion.

From the definition of fundamental mode circuits the present design cannot be measured as a fundamental mode circuit as the input–outputs will go through several transitions before producing the final output. That it is not a Muller circuit working outside the fundamental mode either as internally several transitions will take place as shown in the state diagram. This is similar to cyclic sequential circuit where gate delays are utilized to separate individual states.

4.3 *Recursive Formula for Addition*

Let S_{ji} and C_{ji+1} defines the sum and carry respectively for i_{th} bit at the j_{th} iteration. The initial condition (j = 0) for addition is expressed by:

$$S_i^{\,0} = a_i \oplus b_i$$
$$C_{i+1}^{\,0} = a_i\, b_i \qquad (1)$$

The j_{th} iteration for the recursive addition is expressed by:

$$S_i^{\,j} = S_i^{\,j-1} \oplus C_i^{\,j-1} \quad 0 \le i < n \qquad (2)$$

$$C_{i+1}^{\,j} = S_i^{\,j-1} C_i^{\,j-1} \quad 0 \le i \le n \qquad (3)$$

The recursion is aborted at k_{th} iteration when the following condition is met:

$$C_n^{\,k} + C_{n-1}^{\,k} + \cdots + C_1^{\,k} = 0,\ 0 \le k \le n. \qquad (4)$$

4.4 *Implementation*

A CMOS implementation for the recursive circuit shown in Fig 4..For multiplexers and AND gates using the TSMC library implementations while for the XOR gate we have used the faster ten transistor implementation based on transmission gate XOR to tie the delay with AND gates. The completion detection following is canceled to obtain an active high completion signal (TERM). This needs a large fan-in n-input NOR gate. Therefore a different and more practical pseudo-nMOS design is used.

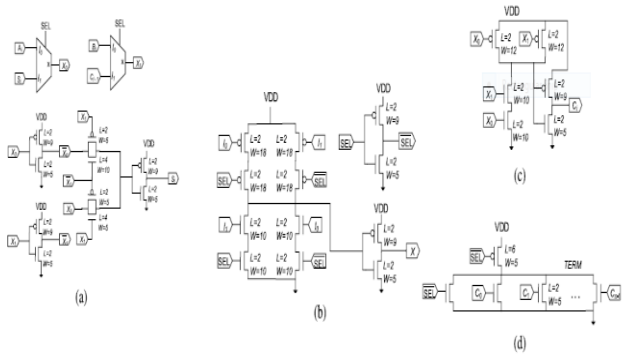

Fig.4. CMOS implementation of PASTA

Using the pseudo-nMOS design the completion unit gets out of the high fan-in problem as all the connections are parallel. The pMOS transistor connected to V_{DD} of these ratioed design performances as a load register resulting in static current drain when some of the nMOS transistors are on simultaneously. In addition to the C_i the negative of SEL signal is also take in for the TERM signal to guarantee that the completion cannot be accidentally turned on during the initial selection phase of the actual inputs. It also avoids the pMOS pull up transistor from being always on.

Hence static current will only be flowing for the duration of the real computation. VLSI layout has also been evaluated for a standard cell environment using two metal layers. The layout space occupies 270 λ × 130 λ for 1-bit resulting in 1.123 Mλ^2 area for 32-bit. The pulls down transistors of the completion detection logic are taken in the single-bit layout while the pull-up transistor is additionally placed for the full 32-bit adder. It is nearly double the area required for RCA and is somewhat less than the most of the area efficient prefix tree Brent–Kung adder (BKA).The design works in a parallel manner for independent carry chain blocks it is different as it employs feedback through XOR logic gates to constitute a single-rail cyclic asynchronous sequential adder.

Cyclic circuits can be more resource efficient than their acyclic counterparts. On the other hand wave pipelining (or maximal rate pipelining) is a technique that can apply pipelined inputs before the outputs become stable. The proposed circuit achieves automatic single-rail pipelining of the carry inputs separated by propagation and inertial delays of the gates in the circuit path. Thus it is efficiently a single rail wave-pipelined approach and quite different from conventional pipelined adders using dual-rail encoding to implicitly represent the pipelining of carry signals.

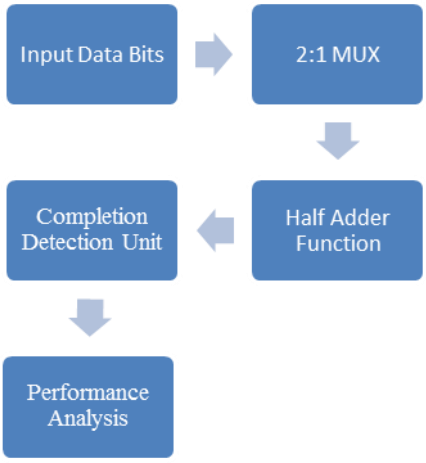

Fig.5. Block diagram of proposed system

5. PROPOSED SYSTEM

5.1 PASTA Design Using DGMOSFET

Multiplexers are device that selects one of several analog or digital input signals and forwards the selected input into a single line. Multiplexers and AND gates are used by library implementations while for the XOR gate it uses the faster ten transistor implementation based on transmission gate XOR to tie the delay with AND gates. Memory-sharing partial parallel architecture achieves a good balance on throughput and

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hardware cost in a large range. The calculation of critical path done which is equal for top and bottom leads to high clock frequency. Encoding is very useful to these LDPC codes because the number of incoming messages to each processing units are uniform across the entire clock cycles. Figure 5 shows the proposed block diagram of PASTA which has the performance analysis block to analyses the performance of the circuit.

5.2 Dual Gate MOSFET

DGMOSFET is designed using lightly doped ultra-thin layers seem to be a very promising option for ultimate scaling of CMOS technology. Excellent short channel effect (SCE) immunity high trans-conductance and ideal sub threshold factor have been provided by many theoretical and experimental studies on this device.

5.3 Structure of Dual Gate MOSFET

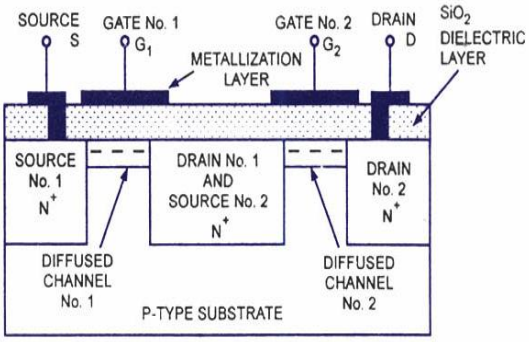

Fig.6. Dual gate MOSFET

The dual gate MOSFET is a form of MOSFET where two gates are fabricated along the length of the channel one after the other. In this way, both gates affect the level of current flowing between the source and drain channel. DGMOSFET is comprised of a conducting channel (usually undoped) surrounded by gate electrodes on both side. This assumes that no part of the channel is far away from a gate electrode. In effect the dual gate MOSFET operation can be considered equal to the two MOSFET devices in series shown in Fig 6. Both gates affect the overall performance of MOSFET operation and output. The dual gate MOSFET has referred as tetrode construction where the two grids control the current through the channel. The different gates control various sections of the channel which are in series with each other.

5.4 Design Challenges

Control of V_T is defined as the value of V_{gs} which is needed to cause surface inversion creating a conducting channel. Due to scaling of V_{dd} we need to have low (~0.2 V) and symmetrical (V_{Tn}= -V_{Tp}) threshold voltages for both transistor types. For DGMOSFETs, V_T is primarily controlled by φ gate. With a unique mid gap material for both NMOS and PMOS symmetrical V_T can be achieved but the value is too large (~0.8 V).

5.5 Fabrication Issues

Fabrication of the DGMOSFET is quite difficult. Alignment of both gates is hard to achieve but it is needed for good device performance. Misaligned gates results in the extra capacitance and loss of current drive. Several different structures have been designed to deal with fabrication issues including planar and quasi-planar structures.

5.6 Advantages

Reduction of I_{off} - Undoped channel eliminates intrinsic parameter fluctuations and controls impurity scattering. Double gate provides for higher current drive capability and has better control of short channel effects.

5.7 Application

There are various applications of DGMOSFET in digital and in analog field such as reconfigurable gates which can perform multiple operations, variable gain amplifiers, high frequency mixers etc.

6. RESULTS

LT spice is an analog circuit simulator with integrated schematic capture and waveform viewer in the tool. It was explicitly written to outperform analogous tools for sale from software companies in the need of being used for in-house IC design as part of Linear Technology Corporation's competitive advantage as a semiconductor company.

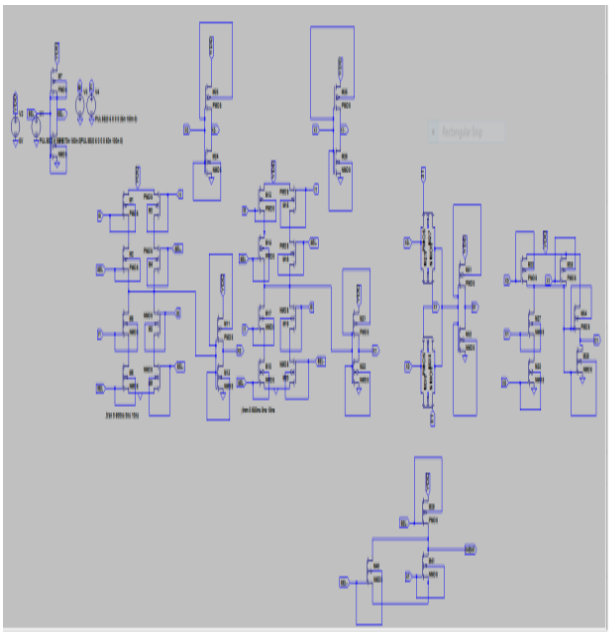

Fig.7. PASTA is designed using DGMOS

The Fig 7 shows the implementation of parallel self-timed adder using DGMOS.

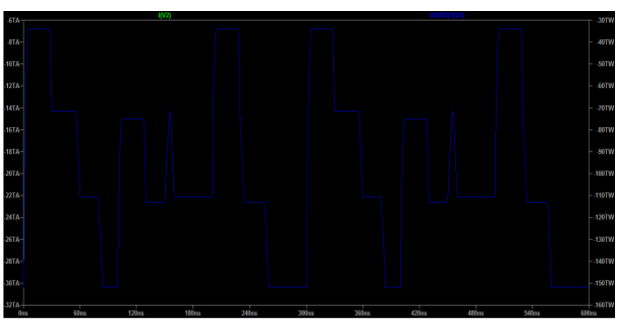

Fig.8. Average power consumption using DGMOS

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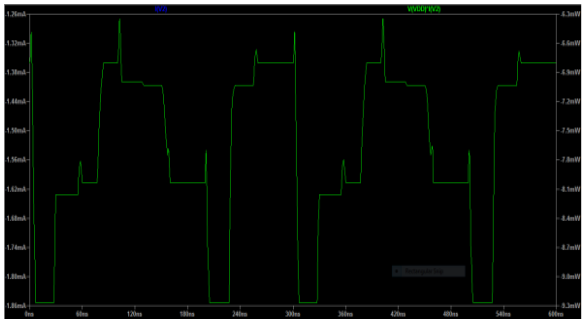

Fig.9. Average power consumption using CMOS

Component	Power consumption
CMOS	-6.802 mw
DGMOS	-151.822 Tw

Thus the parallel self-timed adder is designed using DGMOS which has a better performance over the CMOS. And the result shows thus the power consumption in the circuit is reduced while using dual gate MOSFETs.

7. CONCLUSION

This brief presents an efficient implementation of an adder using DGMOSFET. Initially, the theoretical foundation for a single-rail wave-pipelined adder is established. The design achieves a very simple *n*-bit adder that is area and interconnection-wise equivalent to the performance of simple adder namely the RCA. Thus the DGMOS circuit works in a parallel manner for independent carry chains, and thus provides logarithmic average time performance over random input values. The completion detection unit for the proposed adder using dual gate MOSFET is practical and efficient. Simulation results are used to verify the advantages of the proposed design.

REFERENCES

[1] Rahman.M.Z, Kleeman.L, and Mohammad Ashfak Habib (2014), "Recursive Approach to the Design of a Parallel Self-Timed Adder", *IEEE Transactions on (VLSI) systems.*

[2] Rahman.M.Z and Kleeman.L., (2013) "A delay matched approach for the design of asynchronous sequential circuits," *Dept. Comput. Syst. Technol., Univ. Malaya, Kuala Lumpur, Malaysia, Tech. Rep.* 05042013.

[3] Tinder.R.F (2009), "Asynchronous Sequential Machine Design and Analysis: A Comprehensive Development of the Design and Analysis of Clock-Independent State Machines and Systems" *San Mateo, CA, USA Morgan*.

[4] Choudhury.P, Sahoo.S, and Chakraborty.M (2008) "Implementation of basic arithmetic operations using cellular automaton," *in Proc. ICIT*, pp. 79–80.

[5] Cornelius.C, Koppe.S, and Timmermann.D (2006), "Dynamic circuit techniques in deep submicron technologies: Domino logic reconsidered," *in Proc. IEEE ICICDT*, pp. 1–4.

[6] Weste.N and Harris.D (2005), "CMOS VLSI Design: A Circuits and Systems Perspective Reading", *MA, USA: Addison-Wesley.*

[7] Geer.D (2005), "Is it time for clockless chips? [Asynchronous processor chips]," *IEEE Comput.*, vol. 38.

[8] Riedel.M.D (2004) "Cyclic combinational circuits," Ph.D. dissertation, *Dept. Comput. Sci., California Inst. Technol., Pasadena*, CA, USA.

[9] J. Spars and S. Furber (2001), "Principle of Asynchronous Circuit Design", *Boston, MA, USA: Kluwer Academic.*

[10] Anis.M, S. Member, Allam.M, and Elmasry.M (2002), "Impact of technology scaling on CMOS logic styles," *IEEE Trans. Circuits Syst., Analog Digital Process.*, vol. 49, no. 8, pp. 577–588.

[11] Cheng.F.C, Unger.S.H and Theobald.M (2000), "Self-timed carry-lookahead adders," *IEEE Trans. Comput.*, vol. 49, no. 7, pp. 659–672.

[12] Nowick (1996), "Design of a low-latency asynchronous adder using speculative completion," *IEEE Proc. Comput. Digital Tech.*, vol. 143, no. 5, pp. 301–307.

[13] Liu.W, Gray.C.T, Fan.D, and Farlow.W.J (1994), "A 250-MHz wave pipelined adder in 2-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 29 no. 9 pp. 1117–1128.

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