

# Improved Power Gating Techniques for Reduction of Noise and Leakage Power in VLSI Circuits

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Article Received: 16 February 2017

Article Accepted: 26 February 2017

Article Published: 28 February 2017

## ABSTRACT

Design of complex arithmetic logic circuits considering ground noise, leakage current, active power and area is a challenging task in VLSI circuits. In this paper, a comparative analysis of high performance power gating schemes is done which minimizes the leakage power and provides a way to control the ground noise. The innovative power gating schemes such as stacking power gating, diode based stacking power gating are analyzed which minimizes the peak of ground noise in transition mode for deep submicron circuits. Further to evaluate the efficiency, the simulation has been done using such high performance power gating schemes. Leakage current comparison of NAND gate without power gating and with power gating scheme is done. Finally it is observed that the leakage current in standby mode is reduced by 80% over the conventional power gating. It is also found that in stacking power gating, the ground noise has been reduced by a small extent over the conventional power gating scheme. We have performed simulations using Tanner in a 180nm standard CMOS technology at room temperature with supply voltage of 2.5 V. Finally, a detailed comparative analysis has been carried out to measure the design efficiency of high performance power gating schemes. This analysis provides an effective road map for high performance digital circuit designers who are interested to work with low power application in deep submicron circuits.

Keywords: Power gating schemes, stacking power gating, diode based stacking power gating, leakage power and ground noise.

## 1. INTRODUCTION

With the rapid progress in semi-conductor technology, chip density and operation frequency have increased, making the power consumption in battery operated portable devices a concern [1]. High power consumption reduces the battery service life. The demand for portable electronic devices is growing rapidly and due in large part to the development of wireless communication, is expected to continue to grow.

This demand has generated great interest in low power design. As the technology is reducing further day by day, contribution of leakage power in total power consumption has become comparable to or more than dynamic power consumption. For 180nm technology, it contributes only 10% of the total power while in 90nm technology it is comparable to dynamic power consumption, and for 45nm or technology less than this, leakage power is more than the dynamic power.

In battery operated devices, leakage power may cause serious problem, it reduces the battery life. So, for battery operated portable devices, along with high performance, low leakage power consumption is advised. The most efficient way to reduce the leakage current in standby mode is by using the power gating schemes that uses large transistors, called sleep transistors, in series with the pull up and pull down stacks to cut off the power supply rail from the circuit when the circuit is in standby mode [24].

Ground bounce, also known as simultaneous switching noise or delta noise, is a voltage glitch induced at power ground distribution connections due to switching current passing through either wire substrate inductance or package lead inductance associated with power or ground rails.

## 2. ANALYZED INNOVATIVE POWER GATING SCHEMES

### 2.1 Stacking Power Gating Scheme

Stacking power gating scheme works on two strategies

- 1) Reduction of leakage current by stacking effect
- 2) Reduction of ground noise by controlling the intermediate node voltage.

Strategy to reduce leakage current in standby mode, by taking the advantage of stacking structure leakage current can be controlled in standby mode.

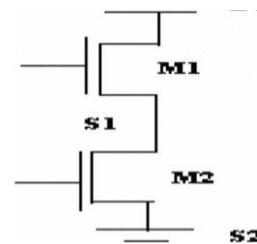


Fig.1. Stacking structure

Here sleep transistors M1 and M2 are stacked. When in standby mode i.e. When M1 and M2 both are off. In this structure firstly, the leakage current is reduced by stacking effect, turning both M1 and M2 sleep transistors OFF. This raises the intermediate node voltage  $V_{GN}$  to positive values to small drain current. In the analyzed scheme, the leakage current is reduced by the stacking effect, turning both M1 and M2 sleep transistors OFF. This raises the intermediate node voltage  $V_{GND2}$  to positive values due to small drain current.

Positive potential at the intermediate node has four effects:

- 1) Gate to source voltage of M1 ( $V_{gs1}$ ) becomes negative.
- 2) Negative body to source potential ( $V_{bs1}$ ) of M1 causes more body effect.
- 3) Drain to source potential ( $V_{ds1}$ ) of M1 decreases, resulting in less drain induced barrier lowering.
- 4) Drain to source potential ( $V_{ds2}$ ) of M2 is less compared to M1, because most of the voltage drops across the M1 in sleep mode. This significantly reduces the drain induced barrier lowering.

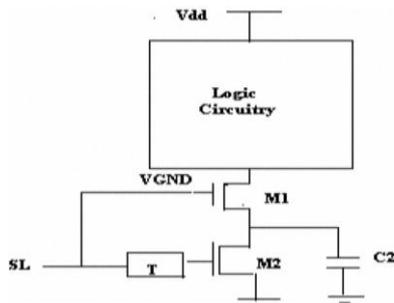


Fig.2. Stacking power gating technique

The expression for the sub threshold leakage current is,

$$I_{sub} = A e^{\frac{q}{nKT}} (V_{gs} - V_{th0} + \gamma V_{bs} + \eta V_{ds}) \left(1 - e^{-\frac{qV_{ds}}{KT}}\right) \quad \text{--- (1)}$$

### 2.2 Strategy to Reduce Ground Bounce Noise

Further, by using this scheme ground bounce noise that occurs during mode transition can be reduced. The proposed strategy is as follows:

- 1) Isolating the ground for small duration during mode transition.
- 2) Turning on the M2 transistor in linear region instead of saturation region to decrease the current surge.

During sleep to active mode transition, transistor M1 is turned ON and transistor M2 is turned ON after a small duration of time (IH). The logic circuit is isolated from the ground for a short duration as the transistor M2 is turned OFF. During this duration, the GBN can be greatly reduced by controlling the intermediate node voltage  $V_{GND2}$  and operating the transistor M2 in triode region. The intermediate node ( $V_{GND2}$ ) voltage can be controlled by

- 1) Inserting proper amount of delay, that is less than the discharging time of the M1 transistor.
- 2) Proper selection of the capacitance C2.

### 3. ANALYSIS OF STATIC POWER GATING SCHEME

Stacking power gating has three modes of operations:

1. Active mode
2. Standby mode
3. Sleep to active mode transition

In active mode, the sleep signal of the transistor is held at logic '1' and both the sleep transistors M1 and M2 remain ON. The equivalent circuit of sleep transistors M1 and M2 is

shown in fig. 3. In this case both transistors offer very low resistance and virtual ground ( $V_{GND}$ ) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage.

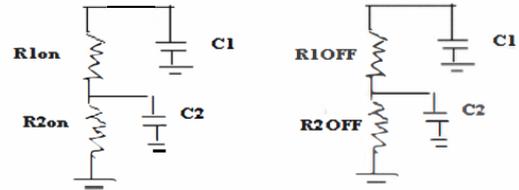


Fig.3. Equivalent circuit of sleep transistors M1 and M2 in (a) active mode, (b) standby mode

So,

$$\text{Voltage across the capacitor } C_1 = V_{C1}(\text{active mode}) = V \frac{R_{2ON}}{R_{1ON} + R_{2ON}}$$

$$\text{Voltage across capacitor } C_2 = V_{C2}(\text{active mode}) = V \frac{R_{1ON}}{R_{1ON} + R_{2ON}} = 0V.$$

### 3.1 Diode based Stacking Power Gating Scheme

If we incorporate the strategy which is operating the sleep transistor as a diode in stacking power gating leads diode based stacking power gating. We can get more ground bounce noise reduction by incorporated strategy. Stacking sleep transistors (S1, S2) are used in diode based stacking power gating scheme shown in fig.4 reduce the magnitude of peak current and voltage glitches in power rails i.e. GBN. In the analyzed diode based stacking power gating scheme, the ground bounce noise is reduced by the following strategies.

- 1) Making the sleep transistor working as a diode during mode transition for some period of time due to this limitation in large transient hence reduction in the peak of GBN.
- 2) Isolating the ground for small duration during mode transition.
- 3) Turning ON the S2 transistor in linear region instead of saturation region. In sleep to active mode transition, initially the transistor M1 is turned ON.

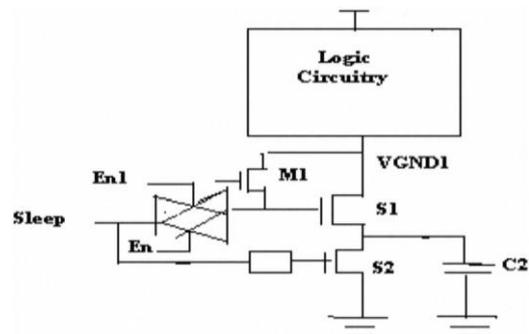


Fig.4. Diode based stacking power gating technique

The intermediate node ( $V_{GND2}$ ) voltage can be controlled by

- 1) Inserting proper amount of delay, that is less than the discharging time of the S1 transistor.
- 2) Proper selection of the capacitance C2.

Leakage current is reduced by the stacking effect, turning both S1 and S2 sleep transistors OFF. This raises the intermediate node voltage  $V_{GND2}$  to positive values due to small drain current.

Positive potential at the intermediate node has four effects:

- 1) Gate to source voltage of S1 ( $V_{gs1}$ ) becomes negative.
- 2) Negative body to source potential ( $V_{bs1}$ ) of S1 causes more body effect.
- 3) Drain to source potential ( $V_{ds1}$ ) of S1 decreases, resulting in less drain induced barrier lowering.
- 4) Drain to source potential ( $V_{ds2}$ ) of S2 is less compared to S1, because most of the voltage drops across the S1 in sleep mode.

This significantly reduces the drain induced barrier lowering.

#### 4. COMPARATIVE ANALYSIS OF SIMULATION RESULTS

Simulation result with power gating scheme in basic NAND gate considering ground bounce noise. The complete simulation setup has been done with basic NAND gate including ground bounce noise model with stacking power gating scheme as shown in Figure 5. Here the effectiveness of the stacking power gating scheme has been demonstrated using NAND gate circuits.

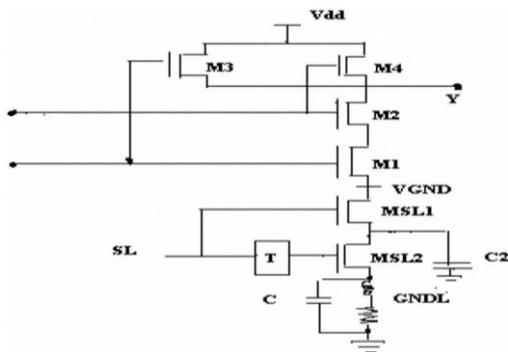


Fig.5. NAND gate circuit with stacking power gating scheme

##### 4.1 Simulation results in standby mode

Leakage current has a strong exponential dependence on VGS and VGD, which leads to input sequence dependence. In the circuit, state of the transistors depends on the input vector. As in the case of 2- input NAND gate, pull down transistors both are turned ON when the input sequence is "11". Hence the leakage current in this case is maximum for 2- input NAND gate. When the input vector sequence is "00" pull down transistors are turned OFF due to stacking effect, hence the leakage current is reduced. All the mentioned results have been simulated under condition that all the logical inputs of NAND gate circuit are held at logic '1'. The worst case condition has been taken where leakage current is maximum, to show the effectiveness of the stacking power gating scheme. To show the improvement in leakage reduction, the stacking power gating scheme has been compared with conventional power gating scheme in terms of leakage current

and power dissipation.

##### 4.2 Leakage Current and power Comparison

The tradeoff between leakage current and power supply in power gating can be easily analyzed from the graph mentioned in figure 6. It shows the leakage current comparison of NAND gate without power gating scheme and with stacking power gating scheme. The leakage current in standby mode is reduced by 80% over the conventional power gating scheme. Figure 7 shows comparison of the average leakage power dissipation in standby mode over the duration of 10  $\mu$ sec, for the conventional and stacking power gating schemes. It is analyzed that variation of leakage power dissipation with supply voltage is minimized in the stacking power gating schemes.

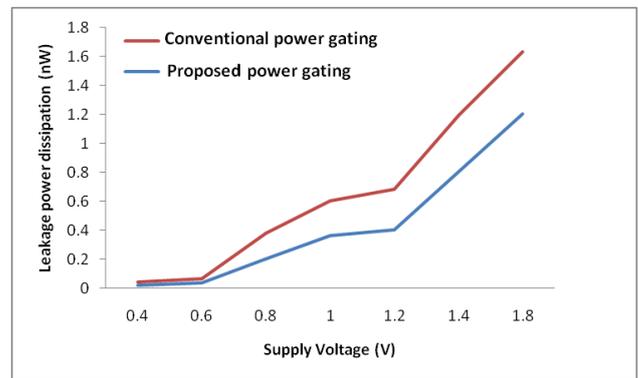


Fig.6. Leakage power comparison

Table 1. Comparison table

Supply Voltage	Existing Power gating	Proposed Power gating
0.4	0.02	0.02
0.6	0.035	0.028
0.8	0.2	0.18
1.0	0.36	0.24
1.2	0.4	0.28
1.4	0.8	0.39
1.8	1.2	0.43

#### 5. CONCLUSION

Power gating is an effective method to reduce leakage current during the circuit sleep mode. However, the conventional power gating technique for minimizing leakage current introduces ground bounce noise during sleep to active mode transition. Here a high performance stacking power gating structure has been presented which will minimize the leakage power as well control the ground bounce noise in transition mode. Stacking power gating technique has been analyzed and the conditions for the important design parameters (i) Minimum ground bounce noise have been derived. As recent trend is towards the nano-scale regime, power gating scheme is mostly used for reduction of leakage current. The ground bounce noise caused by the power gating structure is getting more prominent as the supply voltage is scaled down from 1.5V to 0.5V. The modified stacking power gating scheme reduces the leakage current by 80% and ground bounce noise by 76% compared to the conventional power gating structure. Trade off has been done between leakage current and supply voltage in order to obtain optimum performance. Innovative power gating structures are also presented which reduces the

peak of ground bounce noise in transition mode. The diode based staggered power gating technique, has been implemented on inverter chain. By using this diode based staggered power gating technique, peak of ground bounce noise when it is applied to identical clusters. In case of diode based stacking power gating technique, reduction in peak of ground bounce noise is about 1.5 times compared to stacking power gating technique.

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