Asian Journal of Applied Science and Technology (AJAST)

(Peer Reviewed Quarterly International Journal) Volume 3, Issue 2, Pages 101-104, April -June 2019

Design of Low Power MPSoC Architecture using D-R Method

R.Karthick[1] & D.John Pragasam[2]

[1,2]*Assistant Professor, Sethu Institute of Technology, Virudhunagar, Tamilnadu, India.*

Article Received: 19 September 2018 Article Accepted: 30 January 2019 Article Published: 10 June 2019

ABSTRACT

In this work, static re-configuration allocates time period for an application as well as dynamic re-configuration termed as processing time re-configuration utilizes a dynamic allocation scheme that reallocates hardware at processing time. The benefits of static reconfiguration are remained, and we can achieve an efficient trade-off between time and space. There are two different memories that use the dynamic re-configurable systems. However, implement run-time reconfiguration onto a single context device, the different full memory should be combined to layers within the configuration memory, and each layer is switched inner and outer layer of the FPGA as needed. Mostly, the benchmark performs unique tasks executed by large number of con-current threads.

Keywords: *MPSOC, Low power Design, Wireless communication, Dynamic Allocation.*

1. INTRODUCTION

1.1 Mobile Processor (MP)

Mobile Processor has developed as significant class of VLSI systems [1-4]. Reliability is a developing important challenge in the multiprocessor Systems-on-Chip design. MP represents vital and distinct multiprocessors in branch to complete the necessities of embedded applications uniquely. MP has been in production for higher than multicore processors. Multiprocessor system-on-chip platform gives the high-level of adaptability, performance, reliability and energy efficiency.

The main blocks of the System-on-Chip are: the processing elements responsible for executing the applications, the on-chip memories responsible for storing the application data and instructions, generally, the on-chip interconnect structure responsible for linking the processing elements with the memories and the I/O components.

The tasks are performed on PEs. Based on the type of PEs, two varieties of MP are distinguished:

- Heterogeneous MP which is composed of different types of PEs designed to perform their specific tasks (dedicated accelerators).
- Homogeneous MP which are composed of one type of PE instantiated multiple times where all the elements necessary for the particular application are embedded inside the PE.

Comparing both MP heterogeneous MP0 provide good energy efficiency and performance. Heterogeneous MP target high-performance applications with low-power requirements. Microprocessor architectures may be shown, without loss of common factors, as a part of processing components or nodes which share through a communication loop. Hence, Intermediate nodes may be either software or hardware. Software nodes are having sub systems that should be programmable include one or more common processing unit. Several king of processing unit may be used for the variable sub-systems to realize different components. In order to the architectures, the software part of a hardware node generally includes excess components to raise communication [8-10]. This may varies from easiest bus arbitration to useful memory and parallel Input and Output architectures.

1.2 Optical reconfigurable logic block –Dynamic layer

A functional block diagram of an OR logic block of the VLSI chip modeled as DORGA is presented in below Figure. The Input/Output signals from the switching matrices are applied through some wiring channel and optically reconfigurable Input/output blocks are switched to LUTs through large number of multiplexers [7-12].Each and every OR logic block consists of two 4-input 1 output look-up tables, 10 multiplexers, 12 tri-state buffers, and 2 delay-type flip-flops with a RS function. The I/O signals from the wiring channel are applied through some switching matrices and wiring channels from optically reconfigurable Input/output blocks are transferred to LUTs through eight multiplexers [7-9]. The Look up Tables are used for executing Boolean laws [5-6]. The results of a Look-up-Tables and of a delay type flip-flop are merged to the Look-up-Tables are merged to a multiplexer.

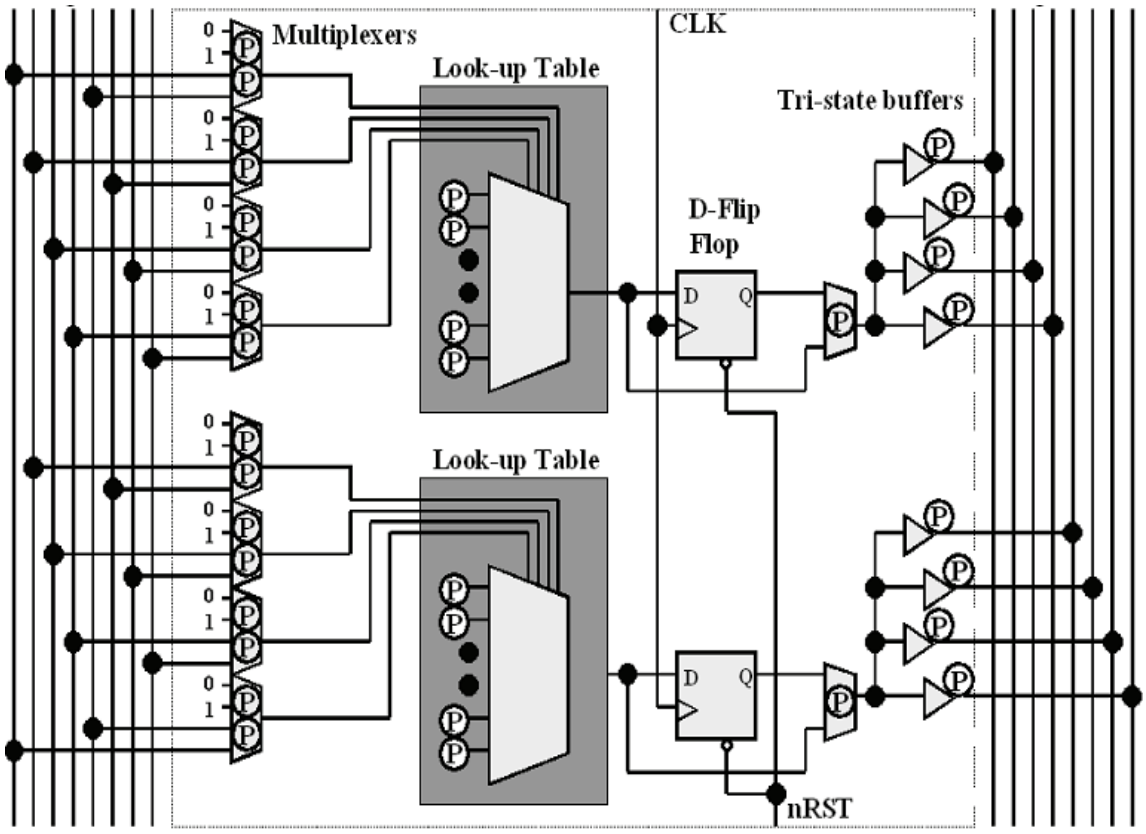


Figure.1 Basic Blocks of an Optically re-configurable block.

The both combinational as well as sequential circuit can be locked by changing the multiplexers in the Field Programmable Gate Arrays. Lastly, outputs of the multiplexers are merged to the channels again through large numbers of3 state buffers. Hence, each Four-input 1-output Look up Tables, multiplexer, and tri-state buffer has 16 photo-diodes, 3 photodiodes, and 1 photodiode, respectively. To execute the circuit clock by clock simultaneously re-configurable devices are essential. From the recent VLSI development, dynamic realization of faster re-configuration and narrow reconfiguration contexts is not possible.

1.3 Look-up-Tables

A Look-up-Tables is the main key factor in our work, it used to reduce power and area. Generally, simple sign-bit exclusion, the Look-Up-Table size is minimized by part at the cost of a principle area overhead. The

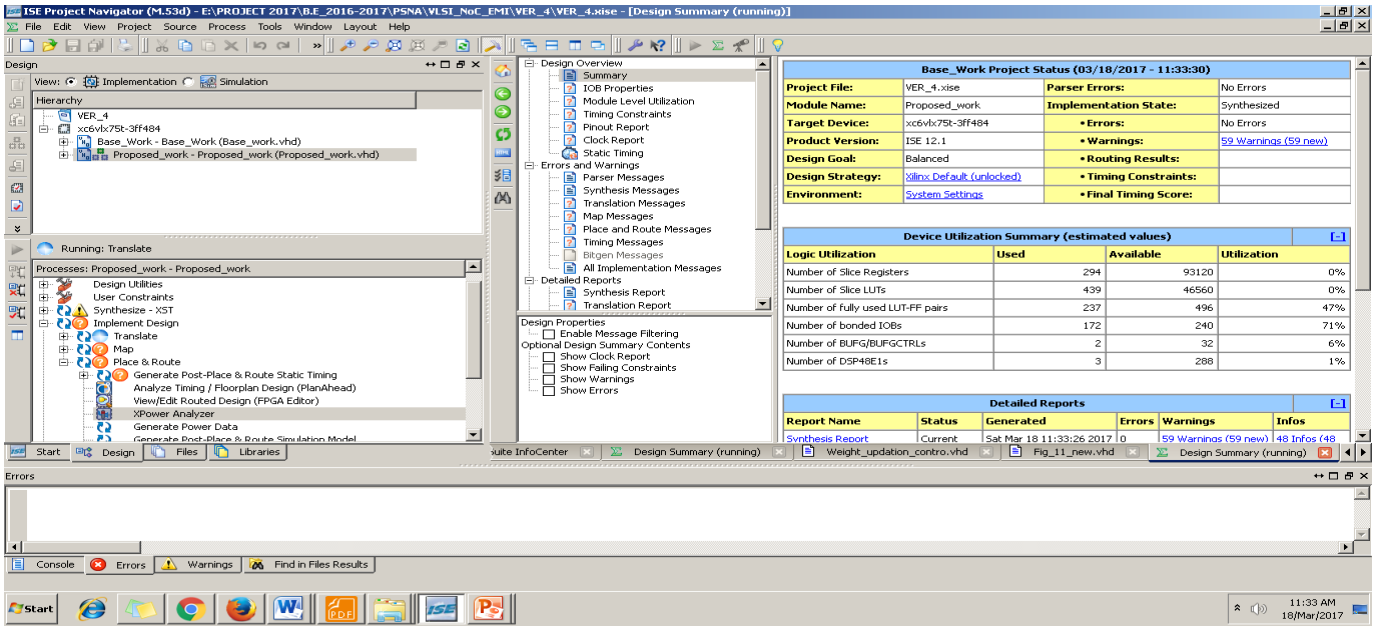
Look-up-Tables are used for executing Boolean laws. The final outputs of an Look-up-Tables and delay type flip-flop connected to the Look-up-Tables are connected to a multiplexer.

1.4 Re-configurable RAM

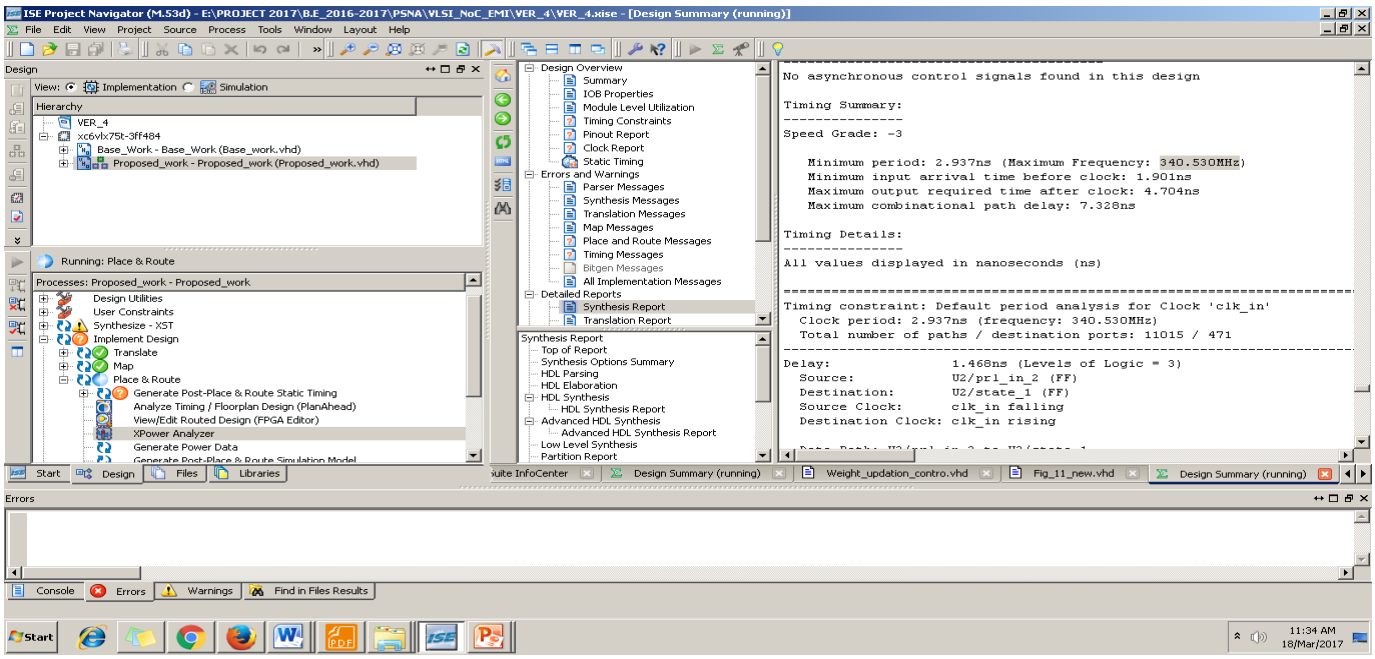
- Here, Static re-configuration plays important and most common used methods for executing applications with re-configurable logic.
- Reconfigurable RAM changes the hardware at very slow rate

2. SIMULATION RESULTS

Area – Proposed Work (294 slices)



Proposed Work-Speed 340.530MHz



 Online ISSN: 2456-883X

In this work, the performance of area, speed and latency improved in the proposed work compare with the existing base work with an architectural level changes in the functional block diagram. Here, overall areas used as 294 slices and speed utilization is about 340.53MHz.

3. CONCLUSION

In this system, we presented a innovative class of MP architecture in which hardware accelerators are shared between processors in such a way to reduce system cost and increase performance. Experimental results have demonstrated that with MP it is possible to obtain the same performance with less logic elements than with MP architecture. In this work, the unique area on the FPGA are shared between cores to implement multiple patterns used for various applications. As future works, we plan to evaluate our dynamically reconfigurable MP MILP model on multithreaded parallel benchmarks.

REFERENCES

[1] Karthick, R and Sundararajan, M: "A Reconfigurable Method for TimeCorrelatedMimo Channels with a Decision Feedback Receiver," International Journal of Applied Engineering Research 12 (2017) 5234.

[2] Karthick, R and Sundararajan, M: "PSO based out-of-order (ooo) execution scheme for HT-MPSOC"Journal of Advanced Research in Dynamical and Control Systems 9 (2017) 1969.

[3]Karthick, R and Sundararajan, M: "Design and Implementation of Low Power Testing Using Advanced Razor Based Processor," International Journal of Applied Engineering Research 12 (2017) 6384.

[4]Karthick, R and Sundararajan, M: "A novel 3-D-IC test architecture-a review," International Journal of Engineering and Technology (UAE)7 (2018) 582.

[5] R.Karthick, P Selvaprasanth, A ManojPrabaharan, "Integrated System For Regional Navigator And Seasons Management," Journal of Global Research in Computer Science 9(4),2018(11-15).

[6] R. Karthick,NSathiyanathan, and M. Eden, "Medical Image Compression Using View Compensated Wavelet Transform" Journal of Global Research in Computer Science 9(9),2018(1-4).

[7] Karthick, R and Prabaharan, A.Manoj and Selvaprasanth, P. and Sathiyanathan, N. and Nagaraj, A., High Resolution Image Scaling Using Fuzzy Based FPGA Implementation (March 15, 2019). Asian Journal of Applied Science and Technology (AJAST), Volume 3, Issue 1, Pages 215-221, Jan-March 2019 . Available at SSRN: https://ssrn.com/abstract=3353627

[8] Karthick, R and Sundhararajan, M., Hardware Evaluation of Second Round SHA-3 Candidates Using FPGA (April 2, 2014). International Journal of Advanced Research in Computer Science & Technology (IJARCST 2014), Vol. 2, Issue 2, Ver. 3 (April - June 2014). Available at SSRN: https://ssrn.com/abstract=3345417.

[9] Karthick, R and John Pragasam, D., Internet of Things based High Security Border Surveillance Strategy (May 24, 2019). Asian Journal of Applied Science and Technology (AJAST), Volume 3, Issue 2, Pages 94-100, Apr-June 2019 . Available at SSRN: https://ssrn.com/abstract= 3394082.