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High Performance VLSI Architecture for Advanced QPSK Modems

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ABSTRACT

The existing system QPSK, 16PSK with the help of conventional modulators as they are relatively fast and area efficient. QPSK MODULATION scheme is used in VLSI architecture for many high speed applications like satellite communication. The proposed architecture is simulated in XILINX software. Our main motive is to produce high performance QPSK module as it supports for satellite communication with more bandwidth and power efficient. Implementing this process in any other module is easy but in VLSI it is a great challenge.

Keywords: QPSK, VLSI, Modulation, Communication, Architecture.

1. INTRODUCTION

As we have seen that VLSI is a technology by which 10000-1 Million Transistors can be fabricated on a single chip. In olden days during the vacuum tube era, the size of Electronic Devices were huge, required more power, dissipated more amount of heat and were not so reliable. So there was certainly a need to reduce the size of these devices and their heat dissipation. After the invention of SSD's, the size and the heat produced by devices was undoubtedly reduced drastically, but as the days passed the requirement of additional features in Electronic Devices increased which again made the devices look bulky and complex. This gave birth to the invention of technology which can fabricate more number of components onto a single chip. As the need of additional features in Electronic Devices aroused, the growth of VLSI Technology has improved.

2. PROBLEM IDENTIFICATION

FSK is a form of constant-amplitude angle modulation similar to standard frequency modulation (FM) except the modulating signal is a binary signal that varies between two discrete voltage levels rather than a continuously changing analog waveform. Consequently, FSK is sometimes called binary FSK (BFSK). FSK Bit Rate, Baud, and Bandwidth: The time of one bit (tb) is the same as the time the FSK output is a mark of space frequency (ts). Thus, the bit time equals the time of an FSK signaling element, and the bit rate equals the baud.

FSK Transmitter is a simplified binary FSK modulator, which is very similar to a conventional FM modulator and is very often a voltage-controlled oscillator (VCO). The center frequency (fc) is chosen such that it falls halfway between the mark and space frequencies. A logic 1 input shifts the VCO output to the mark frequency, and a logic 0 input shifts the VCO output to the space frequency. Consequently, as the binary input signal changes back and forth between logic 1 and logic 0 conditions, the VCO output shifts or deviates back and forth between the mark and space frequencies.

A VCO-FSK modulator can be operated in the sweep mode where the peak frequency deviation is simply the product of the binary input voltage and the deviation sensitivity of the VCO. The FSK input signal is simultaneously applied to the inputs of both bandpass filters (BPFs) through a power splitter. The respective filter passes only the mark or only the space frequency on to its respective envelope detector. The envelope detectors, in turn, indicate the total power in each passband, and the comparator responds to the larger of the two powers. The incoming FSK signal is multiplied by a recovered carrier signal that has the exact same frequency and phase as the transmitter reference. However, the two transmitted frequencies (the mark and space frequencies) are not generally continuous; it is not practical to reproduce a local reference that is coherent with both of them. Consequently, coherent FSK detection is seldom used.

3. PROBLEM SOLUTION

3.1 Quadrature Phase-Shift Keying

QPSK is an M-ary encoding scheme where N = 2 and M= 4 (hence, the name "quaternary" meaning "4"). A QPSK modulator is a binary (base 2) signal, to produce four different input combinations,: 00, 01, 10, and 11. Therefore, with QPSK, the binary input data are combined into groups of two bits, called dibits. In the modulator, each dibit code generates one of the four possible output phases (+45°, +135°, -45°, and - 135°).

3.2 8-PSK

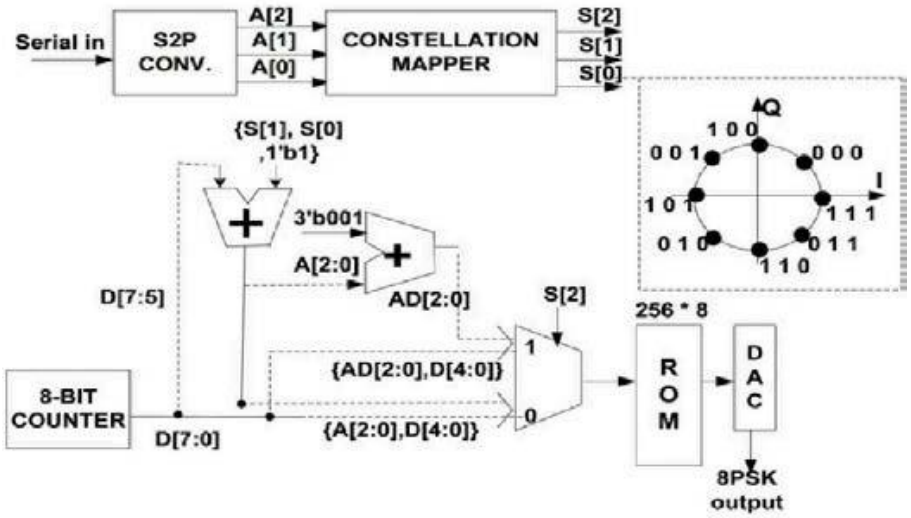

Figure. 1. 8-PSK modulator.

3.3 16-PSK

16-PSK is an M-ary encoding technique where M = 16; there are 16 different output phases possible. With 16-PSK, four bits (called quadbits) are combined, producing 16 different output phases. With 16-PSK, n = 4 and M = 16; therefore, the minimum bandwidth and baud equal one-fourth the bit rate (fb/4). With 16-PSK, the angular separation between adjacent output phases is only 22.5° (1800 / 8). Therefore, 16PSK can undergo only an 11.25°

(1800 / 16) phase shift during transmission and still retain its integrity. For an M-ary PSK system with 64 output phases (n = 6), the angular separation between adjacent phases is only 5.6° (180 / 32).

3.4 16-PSK DEMODULATOR

A 32APSK constellation consists of three rings with 4, 12, 16 symbols on each ring starting from inner ring to outer ring. The outer ring R3 directly represents 16PSK constellation.

4. RESULTS AND DISCUSSION

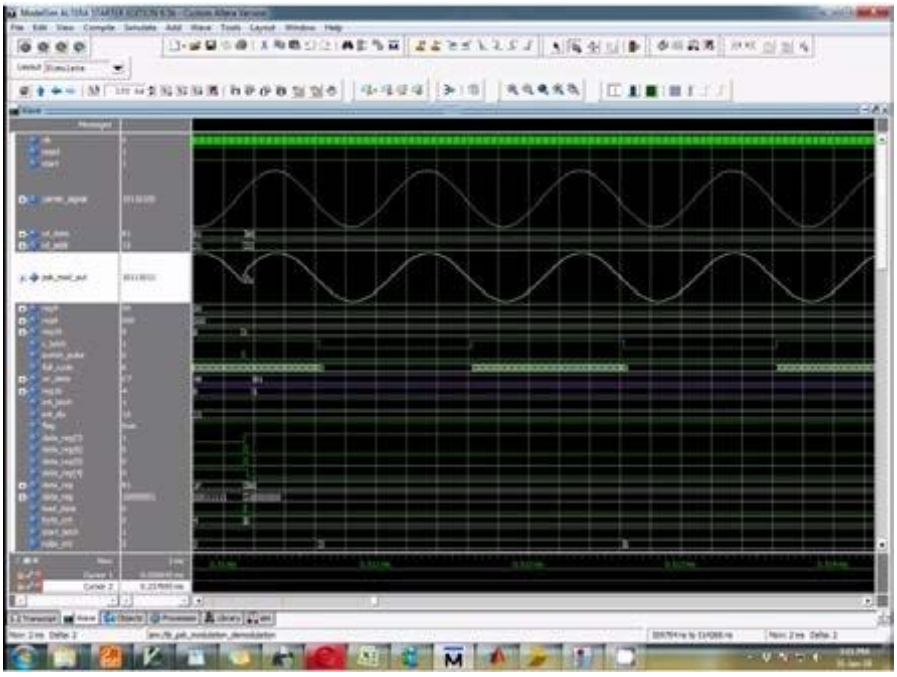

Figure. 2 8-PSK MODULATOR

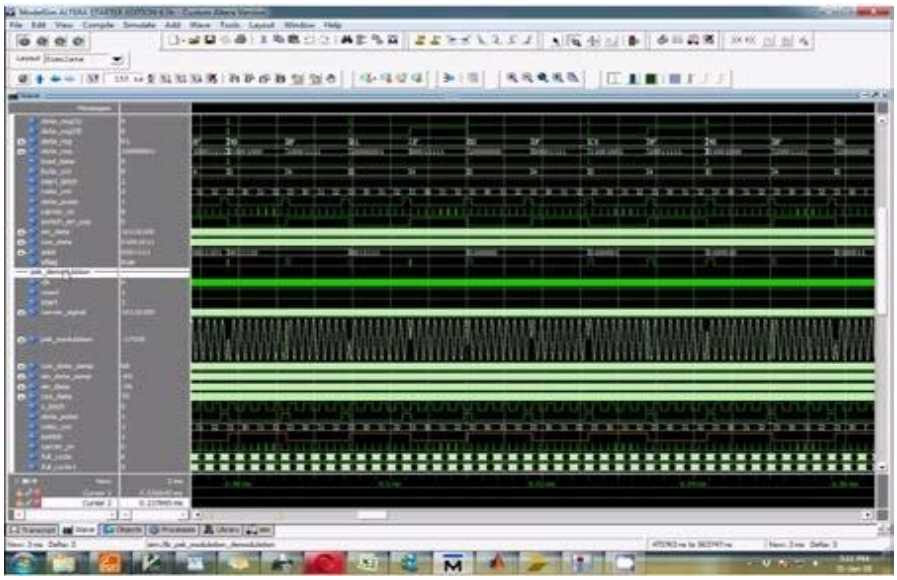

Figure. 3 8-PSK DEMODULATOR

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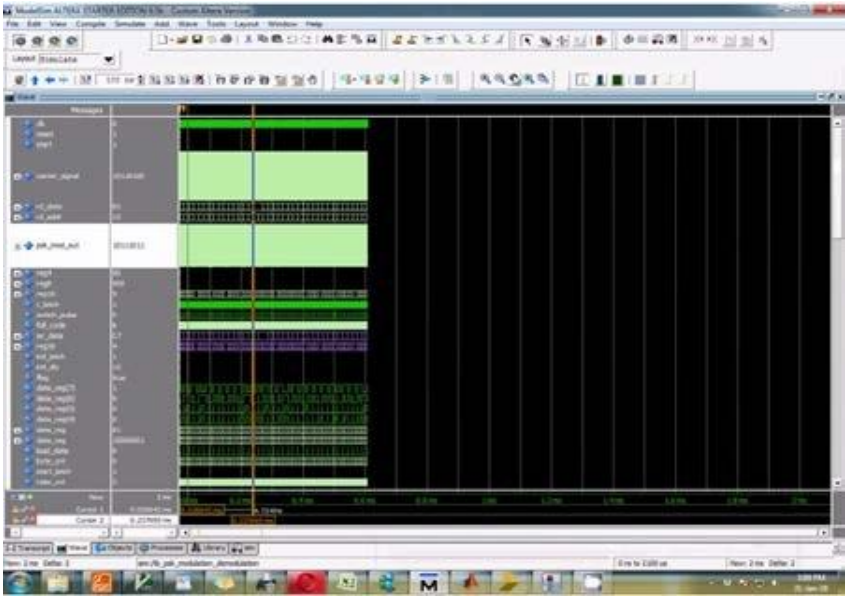

Figure. 4 16-PSK MODULATOR

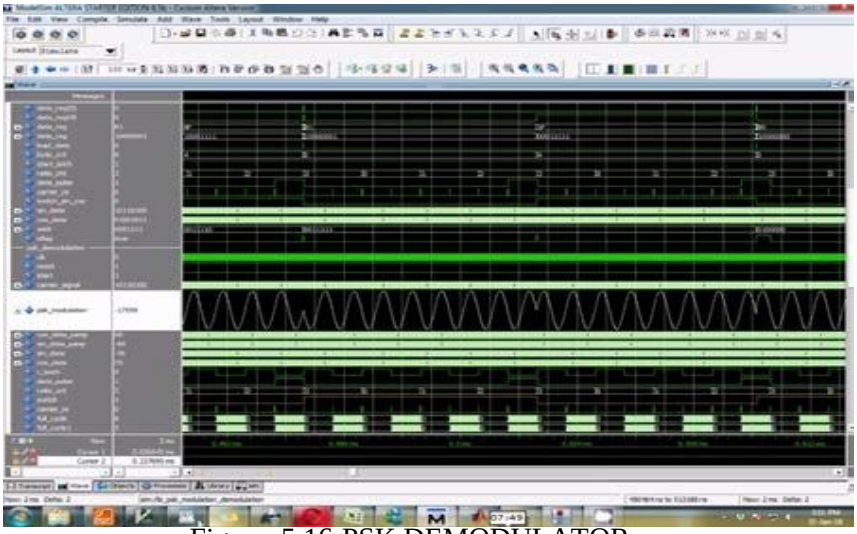

Figure. 5 16-PSK DEMODULATOR

5. CONCLUSION AND FUTERE WORK

In the proposed project, we have simulated 8PSK and 16PSK with the basics of QPSK modulation and demodulation systems for getting the required output. We have used VERILOG coding to simulate our program. The errors are coded and verified using the XILINX software. This Verilog software can run in both in Window 7, 8 and Window 10 operating systems. This project is implemented to create high performance in VLSI with the help of QPSK, 8PSK, 16PSK systems which used for satellite communication.

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