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# Review on an Ultralow Power Subthreshold CMOS Voltage Reference without Requiring Resistors or BJTs

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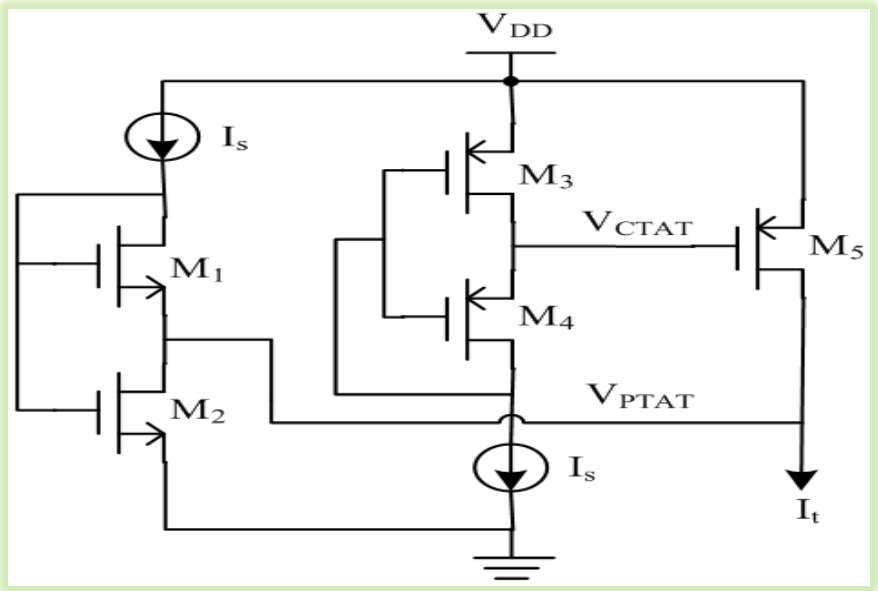
ABSTRACT

This temporary presents a unique ultralow power CMOS voltage reference (CVR) with solely four.6-nW power consumption. within the projected CVR circuit, the proportional-to-absolute-temperature voltage is generated by feeding the outpouring current of a zero-Vgs nMOS semiconductor device to two diode-connected nMOS transistors serial, each of that square measure in subthreshold region; whereas the complementary-to-absolute-temperature voltage is made by exploitation the body diodes of another nMOS semiconductor device. Consequently, low-power operation may be achieved while not requiring resistors or bipolar junction transistors, resulting in little chip space consumption. The projected CVR circuit is invented during a customary 0.18-µm CMOS method. activity results show that the image design is capable of providing a 755 mV typical reference voltage with thirty four ppm/°C from −15 °C to one hundred forty °C. Moreover, the everyday power consumption is just four.6 nor'-west at temperature and therefore the active space is only 0.0598 mm2.

## I. INTRODUCTION

Temperature and voltage insensitive references area unit crucial for a spread of mixed signal and RF systems. With the proliferation of mobile devices and wireless detector networks, reliable voltage references below serious energy constraints have attracted in depth research efforts recently. The design in adopts threshold voltage compensation to come up with two proportional-to-absolute-temperature (PTAT) factors so as to achieve a stronger temperature constant (TC), however needs high supply voltage and huge power dissipation. The circuit in just consumes 2.6 point in temperature and works with offer voltage as low as zero. 45V, however the TC of 142 ppm/° is unacceptable. In the discharge current of a semiconductor unit in sub threshold region is explored to come up with a reference with little TC and additionally with nanowatt or maybe picowatt power consumption. However, in order to minimize the ability consumption, giant resistors square measure needed in that occupy an oversized quantity of chain space. The voltage reference generators in and square measure supported the diode-connected MOS transistor that typically suffer from giant variations and limited operative temperature vary.

A clock circuit is adopted in to control the edge voltage-based reverse bandgap reference, resulting in a reference voltage with glorious TC and accuracy. Still, the microwatt power consumption isn't sufficiently low for ultra low power applications. I associate with degree acceptable current generated from two subthreshold transistors, a temperature insensitive reference is provided at the intermediate purpose of these two transistors. For many of the articles mentioned higher than, either resistors or special devices like low-tension transistors square measure required to implement the reference circuit. Special devices would like additional fabrication steps that will increase the chip value. Although the temperature influence of resistors might be canceled by adopting the magnitude relation of resistance, a exchange perplexity of chip space and power dissipation is brought in by mistreatment resistors.




**Schematic of the proposed PTAT voltage circuit.**

In this temporary, we tend to propose a completely unique structure of CMOS voltage reference (CVR) while not bipolar junction transistors or resistors which achieves a compact space and ultralow power operation. The outpouring current of a subthreshold semiconductor device is employed to supply the PTAT voltage, whereas the body diodes of associate degree nMOS semiconductor device with gate-body shorted accustomed generate the complementary-to-absolute-temperature (CTAT) voltage.

## II. SURVEY ON METHODOLOGIES USED

[1] 0.18µm CMOS PROCESS
[2] 0.35-µm CMOS TECHNOLOGY
[3]TSMC 0.18 µm CMOS TECHNOLOGY
[4] CMOS TECHNOLOGY
[5] 180 nm CMOS TECHNOLOGY
[6] 0.18-µm CMOS TECHNOLOGY
[7] TEMPERATURE COMPENSATION TECHNIQUE
[8] 0.18µm CMOS TECHNOLOGY
[9] 0.13 µm CMOS TECHNOLOGY
[10] SERIES CONNECTION OF TWO NMOS DEVICES

### A) *0.18µm CMOS PROCESS*

The ONC18 process from ON Semiconductor is a low cost industry compatible 0.18 µm CMOS technology manufactured in the United States. This full featured process includes 1.8 V/3.3 V dual gate I/Os, nominal and high value MIM capacitors, resistors, and six levels of metal. A comprehensive design kit offers an expansive core, I/O,

and memory library. Specialty services including stitching and shuttle prototyping are available. ONC18 also serves as a platform for highly integrated **high voltage mixed-signal processes** ideal for many **automotive, industrial, medical,** and **military applications.**

### *B) 0.35µm CMOS PROCESS*

This 0.35-micron CMOS technology offers four metal layers, digital standard cells, an anti-reflective coating and high-efficiency photodiodes, and bulk micromachining. CMC's multi-project wafer service delivers this technology from Austria microsystems through partnership with Circuits Multi Projects (CMP) in France, offering three processes: Basic (see details below), Opto and High voltage.

***The technology is suitable for:***

- Embedded photodiodes, high-density CMOS imaging and optoelectronic detection
- High-voltage operation (maximum 20V gate, 50V operating voltage)
- Mixed-signal designs
- High-speed digital circuits
- For the Basic and Opto processes, bulk micromachining of MEMS structures

### *C)* TSMC 0.18 µM CMOS PROCESS TECHNOLOGY

This 0.18-micron CMOS technology is offered with a robust design kit (with a commercial cell library) that supports RF, analog, mixed-signal and digital design flows, plus various tutorials that use this technology for the design example. CMC's multi-project wafer service delivers Taiwan Semiconductor Manufacturing Company (TSMC) nanometer and micron-scale CMOS technologies through partnership with MOSIS.

The 0.18 µm CMOS (CMC term is CMOSP18) process is suitable for:

- Analog circuits
- Full custom digital circuits
- RF circuits
- Mixed-signal circuits

### *D) CMOS TECHNOLOGY*

The term CMOS stands for "Complementary Metal Oxide Semiconductor". CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs).

***E) 180 nm CMOS TECHNOLOGY***

In this technology there are devices that can be used only up to 1,2V supply, there are a few that can be used up to 1.8V, few up to 2.5V and few up to 3.3Vsupply. This means in this technology you can go for high voltage designs. Say you need to design an amplifier in 3V supply and you only had 1.2V MOSFETs then there will be reliability issues. So you have to use 3.3V MOSFETs for such design.

***F) ONC18: 0.18 μM CMOS PROCESS TECHNOLOGY***

The ONC18 process from ON Semiconductor is a low cost industry compatible 0.18 µm CMOS technology manufactured in the United States. This full featured process includes 1.8 V/3.3 V dual gate I/Os, nominal and high value MIM capacitors, resistors, and six levels of metal. A comprehensive design kit offers an expansive core, I/O, and memory library. Specialty services including stitching and shuttle prototyping are available. ONC18 also serves as a platform for highly integrated **high voltage mixed-signal processes** ideal for many **automotive, industrial, medical**, and **military applications**.

***G) TEMPERATURE COMPENSATION TECHNIQUE***

A fully integrated temperature compensation technique for piezoresistive pressure sensors is presented. The technique is suitable for batch fabricated sensors operable over a temperature range of -40 degrees C-130 degrees C and a pressure range of 0-310 kPa. The implementing hardware for the technique is developed and verified through PSpice and VHDL simulations. The technique is very effective for pressure values below 240 kPa and provides reasonable results for higher pressures. The technique is structurally simple and uses standard IC fabrication technologies.

***H) 0.18μm CMOS TECHNOLOGY***

The ONC18 process from ON Semiconductor is a low cost industry compatible 0.18 µm CMOS technology manufactured in the United States. ONC18 also serves as a platform for highly integrated high voltage mixed-signal processes ideal for many automotive, industrial, medical, and military applications.

***I) 0.13 μm CMOS TECHNOLOGY***

The design of mixed-signal application specific integrated circuits (ASICs) requires a detailed knowledge of the behavior of the technology which exceeds the needs of digital designs. For space applications, with its extended-temperature and radiation environment, the job of the mixed-signal designer is made even more difficult as in most cases commercial foundries do not have or make available data on the behavior of their devices under those nonstandard conditions.

***J) SERIES CONNECTION OF TWO NMOS DEVICES***

N-type metal-oxide-semiconductor logic uses n-type field-effect transistors (MOSFETs) to implement logic gates and other digital circuits. These nMOS transistors operate by creating an inversion layer in a p-type transistor

body. This inversion layer, called the n-channel, can conduct electrons between n-type "source" and "drain" terminals. The n-channel is created by applying voltage to the third terminal, called the gate. Like other MOSFETs, nMOS transistors have four modes of operation: cut-off (or subthreshold), triode, saturation (sometimes called active), and velocity saturation.

## III. CONCLUSION AND FUTURE WORK

An ultralow power subthreshold CMOS voltage reference implemented in a 0.18-$\mu$m CMOS process has been presented in this brief, based on a pure CMOS implementation without requiring any resistors or bipolar junction transistors. A leakage current-based PTAT technique is used and all the transistors are biased in the subthreshold region, which allow significantly low-power consumption with compact chip area consumption. The nanowatt only power consumption of voltage reference with excellent $\sigma$ /$\mu$ performance makes the proposed design a very attractive choice for low-power applications.

## REFERENCES

[1] ] N. Alhassan, Z. Zhou, and E. S. Sinencio, "An all-MOSFET sub-1-V voltage reference with a −51-dB PSR up to 60 MHz," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 3, pp. 919–928, Mar. 2017.

[2] J. Jiang, W. Shu, and J. S. Chang, "A 5.6 ppm/ °C temperature coefficient, 87-dB PSRR, sub-1-V voltage reference in 65-nm CMOS exploiting the zero-temperature-coefficient point," IEEE J. Solid-State Circuits, vol. 52, no. 3, pp. 623–633, Mar. 2017.

[3] I. Lee, D. Sylvester, and D. Blaauw, "A subthreshold voltage reference with scalable output voltage for low-power IoT systems," IEEE J. SolidState Circuits, vol. 52, no. 5, pp. 1443–1449, May 2017.

[4] D. Wang, X. L. Tan, and P. K. Chan, "A performance-aware MOSFET threshold voltage measurement circuit in a 65-nm CMOS," in Proc. IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 4, pp. 1430–1440, Apr. 2016.

[5] Z. Zhu, J. Hu, and Y. Wang, "A 0.45 V, nano-watt 0.033% line sensitivity MOSFET-only sub-threshold voltage reference with no amplifiers," IEEE Trans. Circuits Syst. I, Reg. Paper, vol. 63, no. 9, pp. 1370–1380, Sep. 2016

[6] J. M. Lee, Y. Ji, S. Choi, and J.-Y. Sim, "A 29 nW bandgap reference circuit," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2015, pp. 100–101.

[7] ] Y. Wang, Z. Zhu, J. Yao, and Y. Yang, "A 0.45-V, 14.6-nW CMOS subthreshold voltage reference with no resistors and no BJTs," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 62, no. 7, pp. 621–625, Jul. 2015.

[8] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V subbandgap reference circuits for nanowatt CMOS LSIs," IEEE J. Solid-State Circuits, vol. 48, no. 6, pp. 1530–1538, Jun. 2013.

[9] V. Ivanov, R. Brederlow, and J. Gerber, "An ultra-low power bandgap operational at supply from 0.75 V," IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1515–1523, Jul. 2012.

[10] H. Banba, et al., "A simple CMOS bandgap beference circuit with sub-1-V operation," IEEE J. Solid State Circuits, vol. 34, pp. 670-674, May 2011.