A Low Power Digital Architecture Used for ECG Acquisition System

A.Gowri[1] and Dr.G.Prakash[2]

[1]PG Scholar, Excel College of Engineering and Technology, Namakkal, Tamilnadu, India.
[2]Professor, Excel College of Engineering and Technology, Namakkal, Tamilnadu, India.

ABSTRACT

This paper presents a new power-efficient electrocardiogram acquisition system that uses a fully digital architecture to reduce the power consumption and chip area. The proposed architecture is compatible with digital CMOS technology and is capable of operating with a low supply voltage of 0.5 V. In this architecture, no analog block, e.g., low-noise amplifier (LNA), and filters, and no passive elements, such as ac coupling capacitors, are used. A moving average voltage-to time converter is used, which behaves instead of the LNA and anti-aliasing filter. A digital feedback loop is employed to cancel the impact of the dc offset on the circuit, which eliminates the need for coupling capacitors. The proposed architecture of this paper analysis the logic size, area and power consumption using LTSPICE IV

Index Terms: Antialiasing, area efficient, digital integrated circuit (IC), electrocardiogram (ECG), low power, Voltage to Time converter (VTC), Digital to Current converter (DCC), offset cancellation, sensor .

1. INTRODUCTION

Biomedical devices are more popular. This is due to rapid advancement of Integrated Circuit fabrication. Such devices are being used as wearable or implantable gadgets as well as monitoring equipment. In all these applications, the bio signal is first preconditioned and converted to digital. A patient can be monitored using front end architecture. In this architecture, no analog block, e.g., low-noise amplifier (LNA), and filters, and no passive elements, such as ac coupling capacitors, are used. A moving average voltage-to time converter is used, which behaves instead of the LNA and anti-aliasing filter. A digital feedback loop is employed to cancel the impact of the dc offset on the circuit, which eliminates the need for coupling capacitors

2. EXISTING SYSTEM

The main aim of this project is to make it possible for a patient heart beat monitoring easily and hospitalize doctor's feel it compactable. This goal is achieved by lower power consuming in the circuit. In existing system, a digital signal processor then processes the digital data for Monitoring or diagnosis applications. Biomedical signal acquisition systems typically consist of a low-noise amplifier (LNA), a band pass filter, an analog sample-and-hold, and an analog-to-digital converter (ADC), as shown in Fig. 1(a).

While the architecture shown in Fig. 1(a) is typically used, in some cases chopping technique is used to reduce the impact of the flicker noise, as shown in Fig. 1(b) fabrication. Such devices are being used as wearable or implantable gadgets as well as monitoring equipment. In all these applications, the bio signal is first preconditioned and converted to digital. A digital signal processor then processes the digital data for monitoring or diagnosis applications. Biomedical signal acquisition systems typically consists of a low-noise amplifier (LNA), a bandpass filter, an analog sample-and-hold, and an analog-to-digital converter (ADC), as shown in Fig. 1(a). While the architecture shown in Fig. 1(a) is typically used, in some cases chopping technique is used to reduce the impact of the flicker noise, as shown in Fig. 1(b).
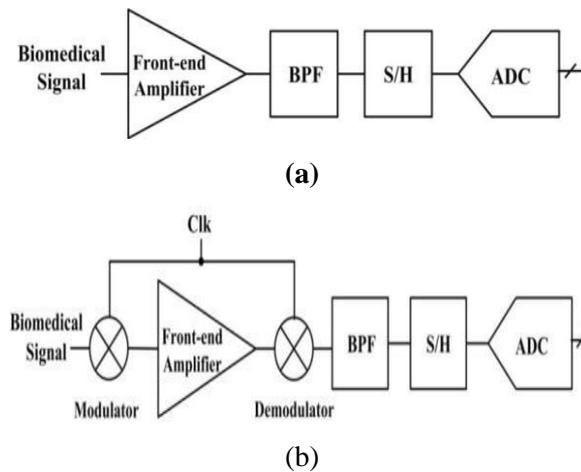
(a)

(b)

Fig. 1. Biomedical signal acquisition system. (a) Conventional based. (b) Chopper based.

3. DRAWBACKS OF EXISTING SYSTEM

Generally, The amplifier; the only analog block that is used, consumes most of the power. Hence, if we can replace the amplifier with an appropriate digital block, the circuit will be more efficient in terms of power. However, there are other issues that should be addressed before moving toward fully digital implementation. Two of these issues are as follows.

1) Removing the DC Offset Voltage of Electrodes without Passive Elements: In these systems, a dc offset voltage as large as 50 mV is associated with the electrodes. Typically this offset is removed by ac coupling the instrumentation amplifier with the electrode. This is not very desirable, since it requires large capacitors.

2) Providing a Solution for Antialiasing Filter: Antialiasing is typically done by low-pass analog filters. Box car sampling technique can be a solution for the fully digital implementation Motivated by the above-mentioned issues, we have designed a new fully digital electrocardiogram (ECG) signal acquisition system. The circuit is designed in 0.18-um CMOS technology and operates by a supply voltage of 0.5V. Using the proposed architecture, the area and power consumption are reduced.

4. PROPOSED SYSTEM ARCHITECTURE

This project is aimed towards the construction and design of an Electrocardiogram system with 0.5V supply. Fig. 2(a) shows the block diagram of the proposed fully digital architecture. In this structure, the processing of the bio-signal is performed in the time and digital domain. Hence, the advantages of digital CMOS technology are utilized. The analog bio-signal coming from the electrode is directly connected to the front-end circuit and is converted to time with a voltage-to-time converter (VTC). From this point on in the circuit, the signal information is in the phase of the VTC output signal. The output of the VTC is applied to the time-mode processing block, in which the anti-aliasing and offset cancellation are done in time domain. Then, a time-to-digital converter (TDC) transfers the time-mode signal into digital domain where other processes (digital filtering, data compression/reduction and so on) are performed. The proposed digital architecture is shown in Fig. 2(b). It consists

of an active electrode, two digital-to-current converters (DCCs), a moving average VTC (MA-VTC), a control logic block, a counter, and a demultiplexer. In this architecture, ac coupling capacitors are removed, and the impact of the electrode offset on the circuit is cancelled via a feedback loop. The technique used for the offset cancellation in conventional bio-signal acquisition systems, an LNA is used after the electrode. In the proposed architecture, this block is removed. In the following text, the proposed architecture is explained.
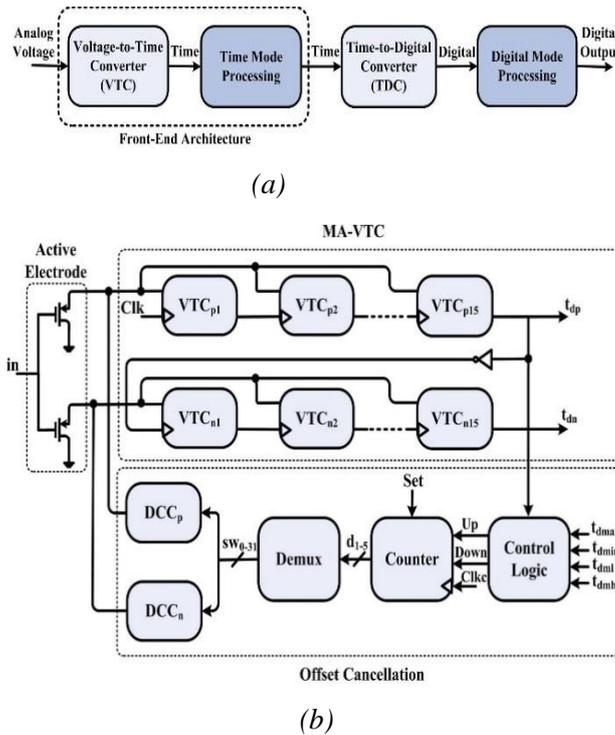

(a)

(b)

Fig. 2. (a) Overall block diagram of the proposed system. (b) Proposed digital front-end architecture

A. Active Electrode

An active electrode is an electrode, in which some active elements are used to reduce the power line interference. Fig. 4 shows two different two wired active electrodes for comparison. The circuit in Fig. 4(a) uses an op-amp, while the one in Fig. 4(b) is implemented using a single transistor. In, important parameters of such electrodes, such as offset, noise, gain, and output resistance, are compared. It is shown in that the circuit in Fig. 4(b) has a superior performance in terms of noise, common mode rejection ratio (CMRR), and power consumption compared with the circuit of Fig. 4(a). However, the offset and the output resistance are worse. Since, in ECG applications, the most important limiting factor is the input noise of the system, we have used the active electrode with a single MOS transistor.

B. Voltage to Time Converter

In the proposed digital implementations, the analog input voltage is converted into a measurable time via a VTC at the first stage. The signal information is now in the delay of clock signal (CLK). The VTC should be designed in such a way that the small amplitude at the voltage *generates* a large enough delay, linearly. In order to have time-domain amplification and acceptable SNR, we have used 15 stages of positive VTC (VTC_p) and 15 stages of

negative VTC (VTC_n). The delays versus input voltage of VTC_p and VTC_n . As the input voltage becomes larger, the delay of VTC_p increases, while the delay of VTC_n decreases. We have used both the positive and the negative VTCs in our design to implement a moving average filter
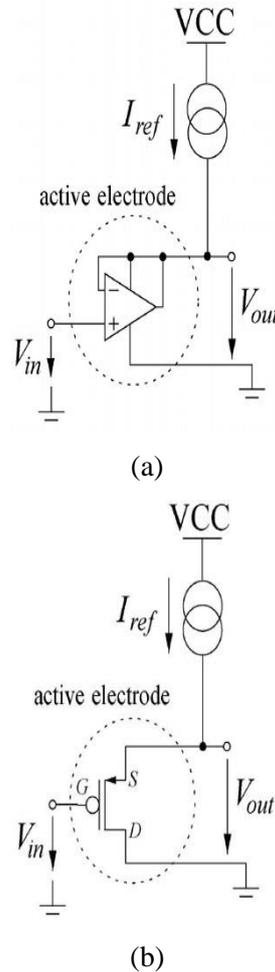

(a)

(b)

Fig.3. Active electrode with either (a) an op-amp or (b) a MOS transistor, both operating as a voltage follower average filter. The cascaded stages of VTCs form delay-line structures.

A major advantage of the delay-line-based structure lies in its all-digital implementation. In addition, the delay line structure introduces time-domain amplification into the design. In particular, the input signal can be amplified in the time domain by simply extending the time window (using more VTC stages). This is in contrast to voltage amplification involving complicated analog amplifiers in the conventional systems.

C. Moving Average Filtering

Since, VTCs work with a clock and are broadband compared with the signal bandwidth, not using an antialiasing filter before VTCs would lead to out-of-band noise aliasing. To prevent aliasing and to avoid having an analog filter in the design, we have developed the structure shown in Fig. 6 for converting the voltage-to-time as well as

antialiasing filtering. In this structure, a chain of 15 positive VTCs are followed by another chain of 15 negative VCTs. This configuration generates a sinc function and is behaving similar to an antialiasing filter.
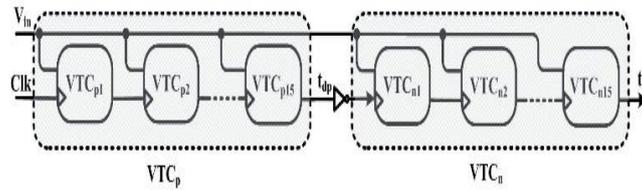

Fig.4.Schematic of the MA-VTC

In another word, the moving average filter is merged with VTCs, and hence we call this block MA-VTC. Therefore the antialiasing filtering is being done without using any passive component or analog amplifier. In antialiasing is done by large area and power hungry analog implementation. The moving average feature of the MA-VTC can be explained intuitively as the following. The CLK signals travels the chain of VTCs. When CLK is passing through the first stage, the delay may be shortened by the noise.
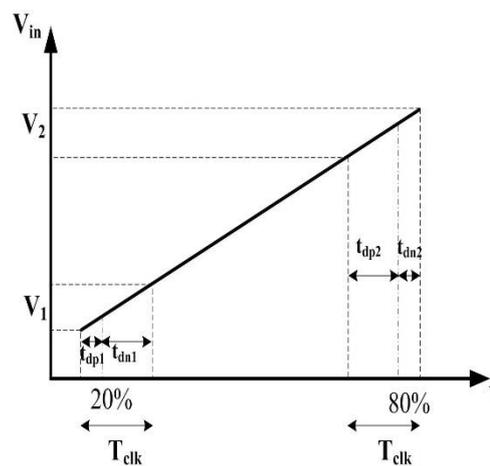

Fig.5.Delays of VTCp and VTCn blocks for two different inputs

This small variation of the delay happens in all stages. At the output of last stage, the overall delay is the sum of the delays of the individual VTCs. As the result the high frequency noise, that the caused delay variations, is cancelled out by the sum operation. This noise cancellation is more effective when the averaging happens during the whole clock period .To achieve this, a negative VTC block succeeds the positive VTC block. This can be explained Fig.6. If the input is small V1, VTCp block will generate a small delay, tdp1 in Fig .6(e.g., 20% of Tclk), and VTCn block will produce a large delay, tdn1 in Fig .6(e.g.,80% of Tclk). The sum of this delay is constant and equal to Tclk.

5. PROPOSED OFFSET CANCELLATION TECHNIQUE

The ECG signal acquisition system should be capable of rejecting the dc polarization voltage of the biopotential electrodes, appearing as a dc offset at the input. This requires a high pass filter (HPF) with a cutoff frequency <1 Hz. This filter requires large capacitors and on-chip implementation of such a filter is not

efficient in terms of area. In the proposed architecture, a new offset cancellation technique is used, in which offset cancellation is done in two stages.
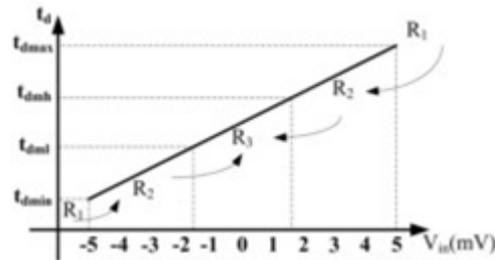

Fig. 6. Characteristic of the VTC_p in the ±5-mV range

First, the impact of the offset on the VTCs are eliminated, such that none of the VTCs are saturated. This is achieved by a digital feedback loop and allows the circuit to take the value of the offset to the digital output. In the second stage, the offset can be removed in the digital domain. In our design, we have assumed an offset voltage of 50 mV. As will become clear later, the proposed system can be easily redesigned to accept even larger offsets.

A. Algorithm

Large amounts of electrode offset make the MA-VTC circuit nonlinear and saturated, to avoid this; we designed MA-VTC circuit, such that it is linear for twice the maximum ECG signal amplitude. The impact of the offset is cancelled by the following algorithm. Fig. 7 shows the characteristics of VTCp. The VTC is linear in the range of -5 to +5 mV. This linear region for which $t_{dmh} < t_d < t_{dmax}$ or $t_{dmin} < t_d < t_{dml}$. Similarly, R_3 shows the region for which $t_{dml} < t_d < t_{dmh}$. Besides R_2 and R_3 regions, R_1 represents regions, in which the input is out of predefined linear range, ±5 mV, of the VTC (i.e., the delay is more than t_{dmax} or less than t_{dmin}). Assuming that the maximum amplitude of the input signal is ±2.5 mV, the delay goes in the R_1 region if the value of the offset exceeds ±2.5 mV. In this case, due to the offset, the circuit behaves nonlinear and may be saturated. When the input falls in the R_1 region, offset cancellation block distinguishes this by comparing t_d with t_{dmax}/t_{dmin}, and reduces the offset, such that the circuit goes back in R_3. The DCC block [Fig. 3(b)] is in the charge of this shift of the operation region. With reducing the offset and putting the circuit in the R_3 region, the operation remains linear. The R_2 region is considered in order to add a hysteresis to the system so that the offset cancellation block does not activate very frequently.

This algorithm is first simulated with MATLAB to verify its functionality (circuit –level simulation results are reported in Section IV). In MATLAB the delay is compared with t_{dmax} and t_{dmin}. If the offset is detected, a voltage is added to or subtracted from the input. At the end, a residual offset of <5 mV may remain, which is tolerable for the circuit. Fig. 8(a) shows the simulation result for a sinusoidal input voltage with 2-mV amplitude and 100-Hz frequency superimposed on a 0.5 Hz, 50-mV sine wave (as an offset voltage). As can be seen, the output is remained in the ±5-mV range.
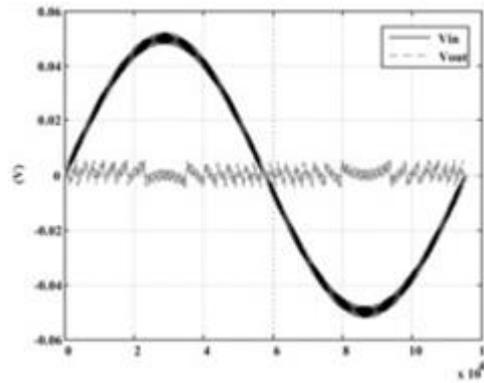
(a)
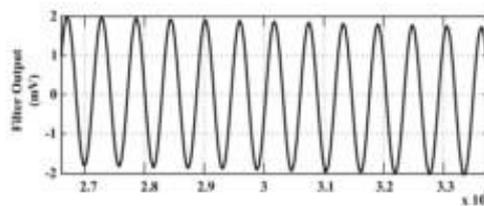
(b)

Fig. 9. (a) Input and output of the digital front end with offset cancellation. (b) Filter output

B. Architecture

The block diagram of the proposed offset cancellation technique is shown in Fig. 10. It contains two 5-bit DCCs control logic circuit, 5 bit counter, and 5-32 demultiplexer (Demux). Since the offset voltage changes very slowly, the frequency of the clock signal used for the counter (Clkc) is ~10 times less than the clock of the rest of the circuit. In this structure, the output delay of the VTC_p block, t_{dp}, is compared with t_{dmax} and t_{dmin} in the control logic block by a time comparator (TC) to determine the operation region of the VTC_p (i.e., R_1, R_2, or R_3).
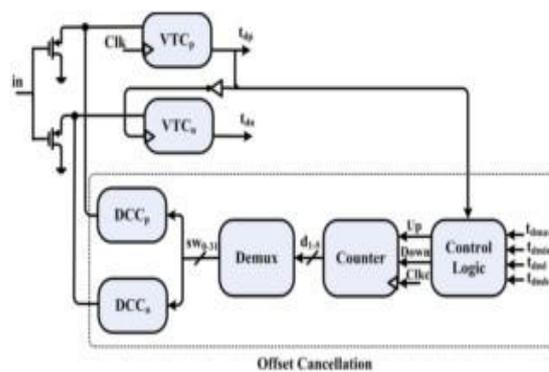

Fig.9. Proposed offset cancellation block diagram

If the delay is more (less) than t_{dmax} (t_{dmin}), the DOWN (UP) signal will be set by the control logic block. The output of the counter changes accordingly and is applied to the Demux, which controls the DCC. The DCC generates a current proportional to its digital input and decreases/increases the input voltage of the VTC_p and

VTC$_n$, (each LSB of the DCC corresponds to 3.125 mV and this is the voltage that is added to/subtracted from the input in each step). This process will continue until the circuit goes into the R_3 region. In this case, the offset value is on the tolerable range of the circuit, (5 mV). Then, offset can be eliminated in digital domain with a simple and low-cost digital HPF

6. CIRCUIT DESIGN

The proposed fully digital front end is implemented in the 0.18-um CMOS technology to evaluate its performance. The supply voltage is 0.5 V, and the circuits are designed to operate in the subthreshold region to reduce the power consumption. Each block of the system and its design challenges is discussed in the following sections.

A. VTC Circuit

Main Control Loop

Fig.10. shows the circuit of the LTC3788-1 uses a constant-frequency, current mode step-up architecture with the two controller channels operating 180 degrees out-of-phase.
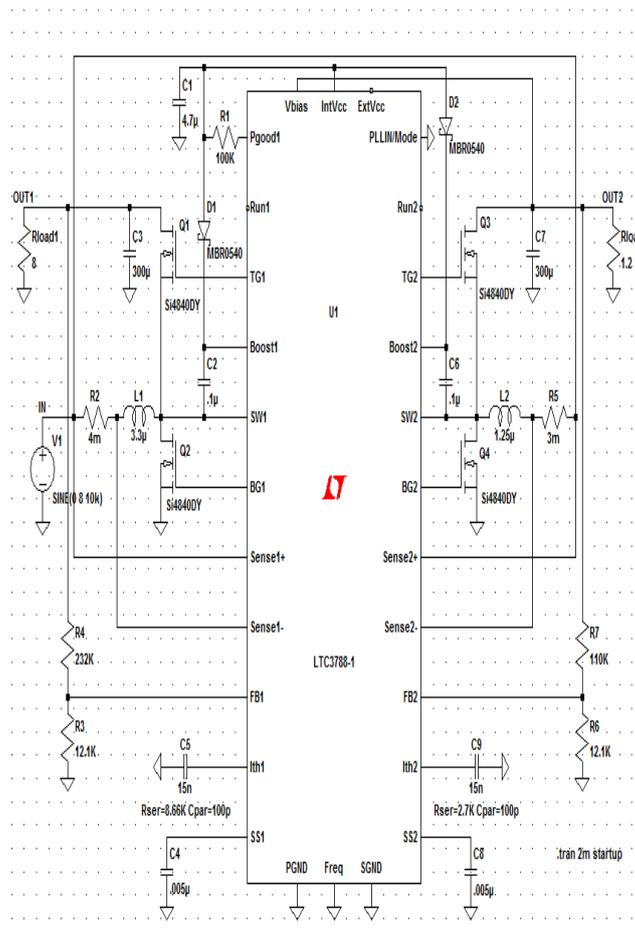

Fig.10. VTC Circuit

During normal operation, each external bottom MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the VFB pin, (which is generated with an external resistor divider connected across the output Voltage , VOUT, to ground) to the internal 1.200V reference voltage. When the load current increases, it causes a slight decrease in VFB relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current. After the bottom MOSFET is turned off each cycle, the top MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

INTVCC/ EXTVCC Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the INTVCC pin. When the EXTVCC pin is left open or tied to a voltage less than 4.8V, the VBIAS LDO (low dropout linear regulator) supplies 5.4V from VBIAS to INTVCC. If EXTVCC is taken above 4.8V, the VBIAS LDO is turned off and an EXTVCC LDO is turned on. Once enabled, the EXTVCC LDO supplies 5.4V from EXTVCC to INTVCC. Using the EXTVCC pin allows the INTVCC power to be derived from a high efficiency external source such as one of the LTC3788-1 switching regulator outputs.

Shutdown and Start-Up

The two channels of the LTC3788-1 can be independently shut down using the RUN1 and RUN2 pins. Pulling either of these pins below 1.28V shuts down the main control loop for that controller. Pulling both pins below 0.7V disables both controllers and most internal circuits, including the INTVCC LDO's. In this state, the LTC3788-1 draws only 8μA of quiescent current. The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. The RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, VIN), as long as the maximum current into the RUN pin does not exceed 100μA. The startup of each controller's output voltage VOUT is controlled by the voltage on the SS pin for that channel. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC3788-1 regulates the VFB voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to SGND. An internal 10μA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond up to INTVCC), the output voltage VOUT rises smoothly to its final value.

Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction (PLLIN/MODE Pin)

The LTC3788-1 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/

MODE pin to a ground (e.g., SGND). To select forced continuous operation, tie the PLLIN/MODE pin to INTVCC. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than INTVCC – 0.5V. When a controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 30% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3788-1 draws. If one channel is shut down and the other channel is in sleep mode, the LTC3788-1 draws only 125μA of quiescent current. If both channels are in sleep mode, the LTC3788-1 draws only 200μA of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous current operation. In forced continuous operation or when clocked by an external clock source to use the phase-locked loop (see the Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry, as it maintains constant-frequency operation independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3788-1 operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3788-1's controllers

can be selected using the FREQ pin. If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to INTVCC, or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to INTVCC selects 535kHz. Placing a resistor between FREQ and SGND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 6. A phase-locked loop (PLL) is available on the LTC3788-1 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC3788-1's phase detector adjusts the voltage (through an internal low pass filter) of the VCO input to align the turn-on of the first controller's external bottom MOSFET to the rising edge of the synchronizing signal.

Thus, the turn-on of the second controller's external bottom MOSFET is 180 degrees out-of-phase to the rising edge of the external clock source. The VCO input voltage is pre biased to the operating frequency set by the FREQ pin before the external clock is applied. If near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of BG1. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency. The typical capture range of the LTC3788-1's PLL is from approximately 55kHz to 1MHz, and is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz. The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling). **Operation When VIN > VOUT.** When VIN rises above the regulated VOUT voltage, the boost controller can behave differently depending on the mode, inductor current and VIN voltage. In forced continuous mode, the loop works to keep the top MOSFET on continuously once VIN rises above VOUT.

The internal charge pump delivers current to the boost capacitor to maintain a sufficiently high TG voltage. In pulse-skipping mode, if VIN is between 100% and 110% of the regulated VOUT voltage, TG turns on if the inductor current rises above a certain threshold and turns off if the inductor current falls below this threshold. This threshold current is set approximately to 4% of the maximum current. If the controller is programmed to Burst Mode operation under this same VIN window, then TG remains off regardless of the inductor current. If VIN rises above 110% of the regulated VOUT voltage in any mode, the controller turns on TG regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the entire chip is asleep (the other channel is asleep or shut down). With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on.

Power Good

The PGOOD1 pin is connected to an open-drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD1 pin low when the corresponding VFB1 pin voltage is not within 10% of the 1.2V reference voltage. The PGOOD1 pin is also pulled low when the corresponding RUN1 pin is low (shut down). When the VFB1 pin voltage is within the 10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V.

Operation at Low SENSE Pin Common Voltage

The current comparator in the LTC3788-1 is powered directly from the SENSE+ pin. This enables the common mode voltage of SENSE+ and SENSE– pins to operate at as low as 2.5V, which is below the UVLO threshold. Figure 1 shows a typical application when the controller's VBIAS is powered from VOUT while VIN supply can go as low as 2.5V. If the voltage on SENSE+ drops below 2.5V, the SS pin will be held low. When the SENSE voltage returns to the normal operating range, the SS pin will be released, initiating a new soft-start cycle.

BOOST Supply Refresh and Internal Charge Pump

Each top MOSFET driver is biased from the floating bootstrap capacitor CB, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. There are two considerations to keep the BOOST supply at the required bias level. During start-up, if the bottom MOSFET is not turned on within 100μs after UVLO goes low, the bottom MOSFET will be forced to turn on for ~400ns. This forced refresh generates enough BOOST-SW voltage to allow the top MOSFET ready to be fully enhance instead of waiting for the initial few cycles to charge up. There is also an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 55μA.

B. DCC Circuit

Main Control Loop

Fig.11.shows the circuit of the LTC3872 is a No RSENSE constant frequency, current mode controller for DC/DC boost, SEPIC and flyback converter applications. The LTC3872 is distinguished from conventional current mode controllers because the current control loop can be closed by sensing the voltage drop across the power MOSFET switch or across a discrete sense resistor. This No RSENSE sensing technique improves efficiency, increases power density and reduces the cost of the overall solution. In normal operation, the power MOSFET is turned on when the oscillator sets the RS latch and is turned off when the current comparator resets the latch. The divided down output voltage is compared to an internal 1.2V reference by the error amplifier, which outputs an error signal at the ITH pin. The voltage on the ITH pin sets the current comparator input threshold. When the load current increases, a fall in the FB voltage relative to the reference voltage causes the ITH pin to rise, which causes the current comparator to trip at a higher peak inductor current value.

The average inductor current will therefore rise until it equals the load current, thereby maintaining output regulation. The LTC3872 can be used either by sensing the voltage drop across the power MOSFET or by connecting the SW pin to a conventional sensing resistor in the source of the power MOSFET. Sensing the voltage across the power MOSFET maximizes converter efficiency and minimizes the component count; the maximum rating for this pin, 60V, allows MOSFET sensing in a wide output voltage range. The RUN/SS pin controls whether the IC is enabled or is in a low current shutdown state. With the RUN/SS pin below 0.85V, the chip is off and the

input supply current is typically only 8μA. With an external capacitor connected to the RUN/SS pin an optional external soft-start is enabled. A 0.7μA trickle current will charge the capacitor, pulling the RUN/SS pin above shutdown threshold and slowly ramping RUN/SS to limit the VITH during start-up. Because the noise on the SW pin could couple into the RUN/SS pin, disrupting the trickle charge current that charges the RUN/SS pin, a 1M resistor is recommended to pull-up the RUN/SS pin when external soft-start is used. When RUN/SS is driven by an external logic, a minimum of 2.75V logic is recommended to allow the maximum ITH range.
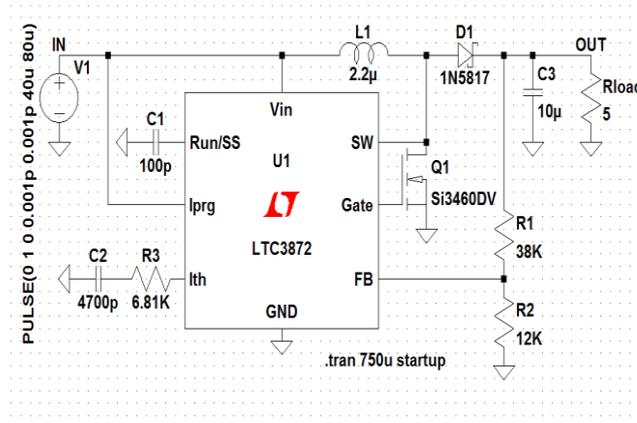

Fig.11 DCC Circuit

Light Load Operation

Under very light load current conditions, the ITH pin voltage will be very close to the zero current level of 0.85V. As the load current decreases further, an internal offset at the current comparator input will assure that the current comparator remains tripped (even at zero load current) and the regulator will start to skip cycles, as it must, in order to maintain regulation. This behavior allows the regulator to maintain constant frequency down to very light loads, resulting in low output ripple as well as low audible noise and reduced RF interference, while providing high light load efficiency.

7. SIMULATION RESULT

The proposed architecture is implemented in 0.18-um CMOS technology. Fig. 12 shows the frequency response of the front end. The dots in this figure represent the simulation results, and the solid line shows an ideal sinc function. As can be seen, the frequency response of the front end closely resembles the sinc function with f_s = 57.8 kHz.

To show the behavior of the offset cancellation block a 1 kHz 2-mV sinusoid voltage superimposed on a 5 Hz 50mV sin wave is applied to the input. The input and the recovered output voltages are shown in Fig. 13. As can be seen, at point A (V_{in} = 5.5 mV), the delay of the VTC_p is 8.8641 us, which indicates the operation region of the VTC is in R_1 region. The offset cancellation mechanism has brought back the operation region to R_3. The circuit operates in region R_3 and moves to region R_2 as the offset of the input increases. When the

input offset voltage reach 11mV, the offset cancellation circuit detects this shift and cancels the impact of the input offset (point B). After recovery, the whole signal is present in the output digital signal and digital filtering should be done finally.

In order to check the performance of the front end an ECG signal from the MIT-BIH arrhythmia database record 101 is applied to the system. Fig.14 . shows the original (Vin) and
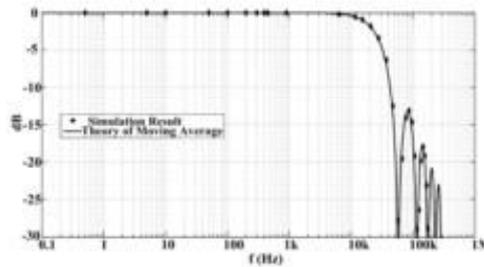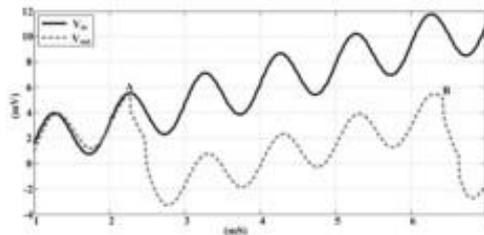

Fig. 12. MA-VTC filter result

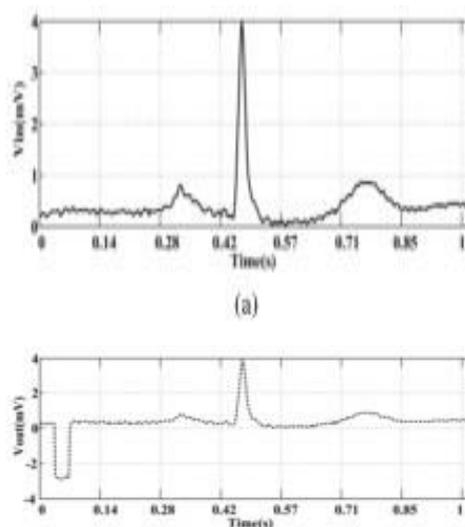Fig. 13. Input and recovered output of the front end with offset cancellation.

(a)

Fig. 14. Record number 101 of the MIT-BIH database. (a) Original signal. (b) Recovered signal

The recovered signals (V_{out}). As can be seen, at the beginning the offset cancellation circuit is acting and setting the output of the DCCs and after this transition

TABLE IV

SUMMARY OF SIMULATED SYSTEM CHARACTERISTICS

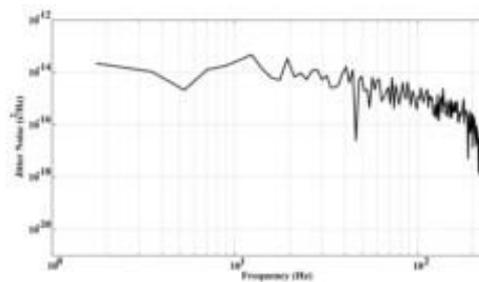| Parameter	Values
Technology	$0.18\mu m$
Supply Voltage	0.5V
VTC Gain	$176\mu s/V$
Rms Jitter	5ns
SNR	42dB
THD	53.5dB
PSRR	67.7dB
Power Consumption	274nW

Fig.15 Jitter noise power spectral density

time the output signal is reliable Fig le. The overall performance parameters of the front end are shown in Table IV. The VTC gain is defined as the ratio delay variation at the output of the VTC blocks and the input voltage range. In order to explore the noise performance of the front end, the jitter is obtained at the output of the front end. The noise power spectral density is shown in Fig. 15 and a jitter noise of 5 ns and SNR of 42 dB are obtained. Depending upon the required resolution this amount of noise may be large. Since there is a tradeoff between power and noise, in order to reduce the noise more power should be burnt. Using the proposed PSRR enhancement circuit in this paper leads to the PSRR of 67.7 dB. The power consumption of the overall front end is 274 nW and is noticeably less than other mixed-signal ECG front-end circuits. This can be considered as one of the main advantages of the proposed fully digital architecture.

8. CONCLUSION

In the expectation of the future dominance of digital CMOS technology, we have implemented a fully digital front-end architecture for an ECG acquisition system. In this system, passive elements, LNA, and analog filters are not used. The proposed digital architecture is compact and power efficient compared with the other analog implementations of these systems. A new offset cancellation technique is used, which reduces the 50-mV offset voltage to <5 mV and makes it tolerable for the system. A moving average mechanism embedded into the TC of the front end eliminates the need for antialiasing filter. The proposed architecture is simulated in 0.18-um CMOS technology at 0.5 V supply voltage. The simulated power consumption is 274 nW.

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