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Power Optimization Techniques – A Study

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ABSTRACT

In digital design, power optimization is a critical concern for battery life, reliability and yield. Power optimization technique is an electronic design automation to optimize (reduce) the power dissipation and to obtain high performance and energy efficiency in digital design while preserving the functionality. For optimization technique Static Random Access Memory is used for reducing power dissipation in digital design. SRAM is one of the largest components in system-on-a-chip and high performance VLSI circuits. Currently different types of SRAM are used. In order to limit the power dissipation conventional 6T-SRAM is used. In this survey paper, different existing optimization techniques are used to reduce power dissipation, increase process variation and variability issues are presented. The Optimization techniques discussed are Power Dissipation Techniques, Mitigation Techniques, and Modelling Techniques. The Modified Hybrid empirical model is used for optimizing and has been simulated by 45nm technology using tanner EDA tool.

Keywords: Optimization, 6T-SRAM, low power dissipation, high performance, energy-efficient

1. INTRODUCTION

Recently reduction of Power dissipation in memories is the major factor in VLSI circuit to achieve low power and high performance. The important parameter on which memory designers have to optimize the design is power, area, speed, performance and increasing memory capacity. To meet the challenges conventional 6T-SRAMs are used in design. SRAM are capable to store large quantities of digital information which is needed in today's system-on-chip and to obtain high performance in VLSI circuits. SRAMs are the main contributor to overall power consumption and vulnerable component to effect of power variations [7]. The primary objective of low power and high-performance circuit design is to increase battery lifetime, long term device reliability, reduce weight and system cost. Increasing the demand for large storage capacity in memories has made technology scaling to reduce the supply and threshold voltages and retention of transistor off-current which causes the standby power of memory to increase. In digital circuits the power dissipation can by reduced using several optimization techniques. The Standby Leakage suppression Techniques, Techniques to reduce retention current for SRAM memories are used for power optimization. Mitigation Techniques are used to improve functional performance by neutralizing positive impacts. Modelling Techniques are used to obtain energy efficient by optimizing the negative impact of process and operation variations [6].

2. SIX TRANSISTOR STATIC RANDOM ACCESS MEMORY (6T-SRAM):

The six- transistor-cell static random access memory is the conventional choice for most on-chip memory designs. Conventional 6T-SRAM is used normally in the array structure which has less layout area. A 6T-SRAM cell consists of two cross coupled two access transistors. The access transistors are connected to the word line at their respective gate terminals, and the bitlines at their source/drain terminals. The word line is used to select the cell while bit lines are used to perform read or write operations on the cell. Internally holds the stored value on one side

and its complement on the other side. The two complementary bit lines are used to improve speed and noise rejection [5].

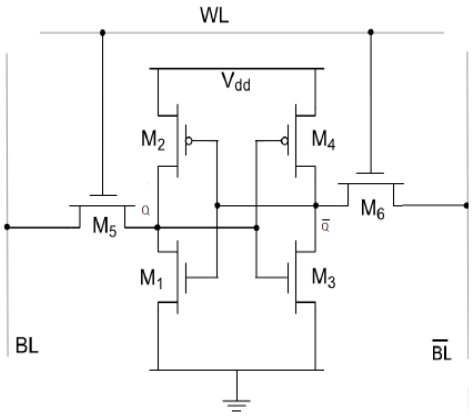

Figure 1.1 6T-SRAM

When power is applied 6T-SRAM provides permanent data storage to different components of leakage current.

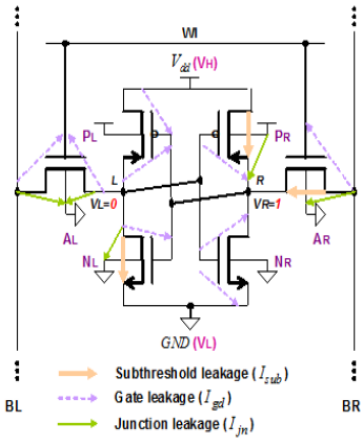

Figure 1.2 Different components of SRAM cell leakage

The 6T-SRAM cell is the important choice for most on –chip memory. It consists of two cross coupled inverters, which forms a positive feedback for two possible states.

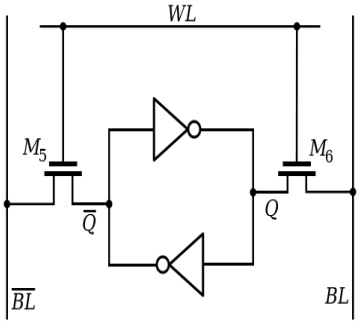

Figure 1.3 6T-SRAM cell

3. DIFFERENT OPTIMIZATION TECHNIQUES

To design low power, high performance and energy efficient VLSI circuit using 6T-SRAM various techniques are used. They are:

1. Power dissipation Techniques.
2. Mitigation Techniques.
3. Modelling Techniques.

3.1. Power Dissipation Techniques

The power consumption is becoming major concern in VLSI circuit design. To reduce power dissipation and energy efficient is a challenging job for low power designer. The Power Dissipation of 6T-SRAM is dominated by dynamic dissipation due to switching activity in CMOS circuits [1]. The sub-threshold leakage in 6T-SRAM is the main reason to increase the leakage power. To reduce power dissipation in SRAM memories techniques used are Leakage Suppression Techniques can done by inserting extra resistance in the leakage path, reducing the supply voltage. Techniques to reduce the retention current in existing SRAM memories can done by disconnecting unused memory blocks, using body biasing to increase the thresholds [4] .

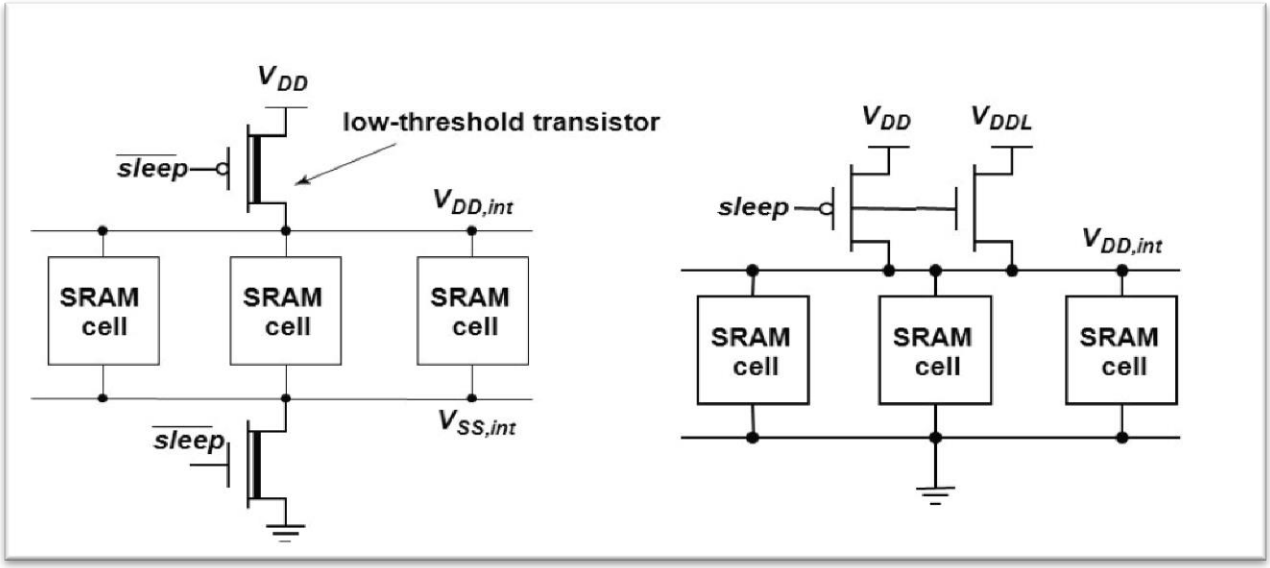

Figure 1.4 Leakage Suppression Techniques.

3.2. Mitigation Techniques

Mitigation Techniques are used in the design to optimize the positive impact of process and operation variations. These techniques are used reduce SRAM layout to obtain high performance by minimizing size width of bitlines. When widening the bitline it reduces current density the mitigation technique is used. Leakage control techniques are used in CMOS processes to obtain the requirements of high performance during active period and low leakage during standby mode [4]. In SRAM low- threshold voltage device is used in cross-coupled inverters to reduce leakage current in write access transistors. The high-threshold voltage device is used in read port to obtain high-performance. The threshold voltage of the device is reduced to control the speed and leakage [5].

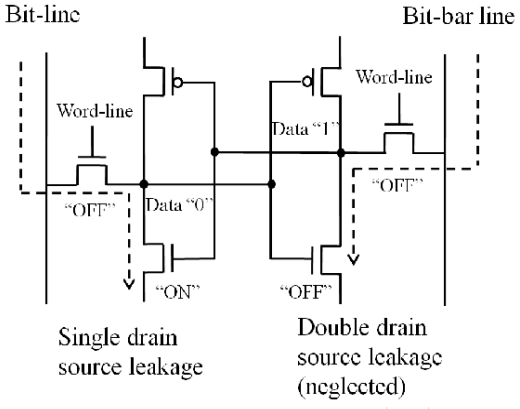

Figure 1.5 Sub-Threshold leakage control technique

The sub-threshold leakage current depends upon the data stored in the cell. When SRAM cell stores '0', due to high voltage on bit bar NMOS transistor is turned ON. The access transistor is switched to limit the sub-threshold leakage and this is single drain source leakage. When the access transistor and NMOS transistor is turned off then it is double drain source leakage. The double source leakage and inverse leakage are neglected when the write operation is small [4].

3.3. Modelling Techniques

Modelling Technique is used in the design to optimize negative impact of process, operation, an environmental and aging variation which allows the SRAM to improve its energy efficient. There are various models used such as chip-area models, power/leakage models, access-time models and failure probability models. To optimize impact on process variation new technique are also used. They are adaptive body biasing or chip-by-chip resource resizing in micro architectural designs. This technique is used predict the delay and delay variability by threshold voltage, channel length, supply voltage variations. The leakage and leakage variability are predicted from SRAM size and shape, area and speed constraints, number of columns and word size in modelling technique. To obtain high energy efficiency of a SRAM both power reduction and performance improvements are calculated by using the metric energy-delay product [8]. A metric that combines a measure of performance and energy is the energy-delay product:

$$EDP = PDP \times tp$$

Where

EDP – Energy-Delay Product.

PDP – Power Delay Product.

tp - propagation delay of a logic gate.

4. VARIABILITY ISSUES AFFECTING SRAM POWER

Variability issues play an important role in performance improvements and energy consumption. The designers use variability-aware memory management techniques to reduce power dissipation to meet the challenges such as high-performance requirements and energy efficient [2].

Variability issues impacting SRAM power are:

1. Impact on supply voltage (Vdd).
2. Impact on temperature.
3. Impact on negative bias temperature instability.
4. Impact on Electromigration.
5. Impact of memory and soft errors.

5. OVERVIEW OF OPTIMIZATION TECHNIQUES

The analysis of power dissipation technique, mitigation technique and modelling technique are explained. Based on the choice of the supply voltage, transistor threshold and device sizes the optimal architecture of data-path, speed, area and power can be traded off. In power dissipation technique the power consumption is reduced when supply voltage is lowered. Threshold voltage is increased to reduce the leakage component. Low-threshold devices and high threshold devices are used in the technique for leakage suppression, timing-critical path and data storage. In mitigation technique impact on threshold voltage is lowered to obtain high-performance. In modelling technique impact on increasing threshold voltage of high threshold voltage devices in optimal design increases the energy efficiency. Variability issues play an important role in performance boosting and energy reduction.

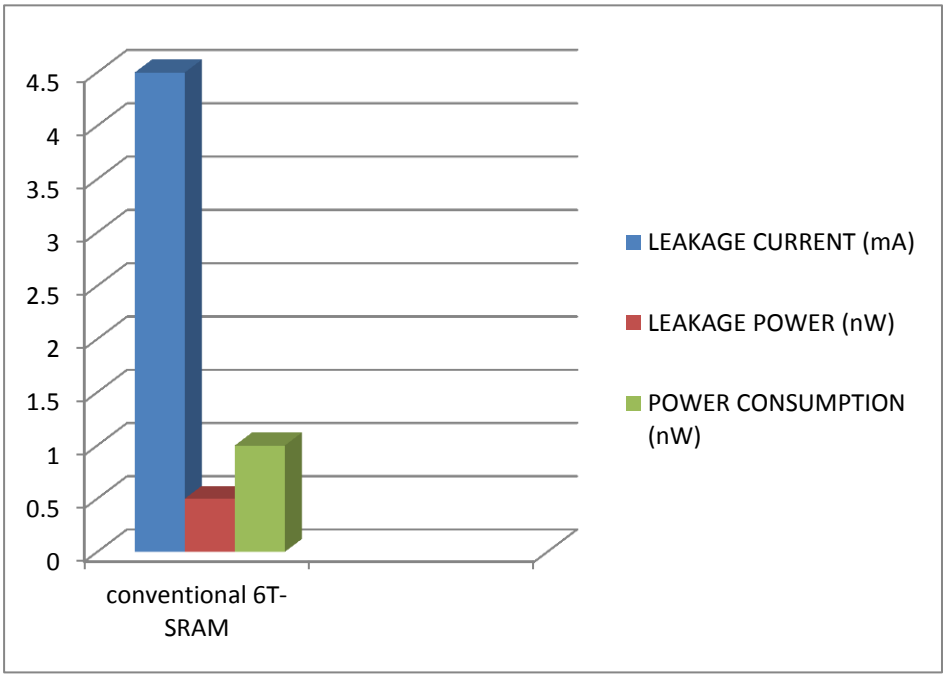

Figure 1.6 Overview of Optimization Technique for 6T-SRAM

6. CONCLUSION

The analyses of some optimization techniques are discussed to reduce power, area and delay to obtain high-performance and energy efficiency in 6T-SRAM. The power dissipation technique is preferable for power reduction. The mitigation technique is preferred for less area to obtain high-performance. The modelling technique

is preferred to overcome the negative impact of process and operation to obtain maximum energy efficiency. There are several other techniques such as adaptive body bias and chip-by-chip resource resizing in micro-architectural structures to reduce dynamic power reduction and study on the same and simulation results must be verified by Monte Carlo will be carried out in future work

REFERENCES

[1] Samandari-Rad, M.Guthaus, and R.Hughey O.Weber, E.Josse, J.Mazurier, and M.Haond, "Static and dynamic power management in 14 nm Fdsoi technology," in Proc. ICICDT, Leuven, France, Jun 2015, pp. 1-4.

[2] J.Samandari-Rad, M.Guthaus, and R.Hughey, " Confronting the variability issues affecting the performance of next-generation SRAM design to optimize and predict the speed and yield" IEEE Access, vol 2, pp. 577-601, Jun 2014.

[3] Z.Guan, M.Marek-Sadowska, and S.Nassif, " Statiscal analysis of process variation induced SRAM electromigration degradation," in proc. 15th Int, symp. Quality Electron. Design (ISQED). Santa Clara, Ca.USA, Mar.2014, pp.700-707.

[4] A.R.Subramaniam, R.singhal, C.C.wang and Y.Cao, "Leakage reduction through optimization of regular layout parameters, "Micro electron. J., vol, no. 1, pp. 25-33, Jan 2012.

[5] J.Samandari-Rad, M.Guthaus, and R.Hughey, "VAR-TX: A variability- aware SRAM model for predicting the optimum architecture to achieve minimum access-time for yield enhancement in nano-scaled CMOS," presented at the 13th Int. symp. ISQED, Santa Clara, CA, USA, Mar.2012.

[6] M.Kumar, M.A.Hussain, and L.L.K.Singh, "Design of a low power high speed ALU in 45nm using GDI technique and its performance comparsion," in Proc. 2nd Int Conf.commun, Comput, Inf, Sci., 2011, pp.458-463.

[7] J.M. Rabaey, A.Chandrakasan, and B.Nikolic, " Designing memory and array structures." In Digital Integrated Circuits, 3rd ed, Englewood Cliffs, NJ, USA: Prentice Hall, 2008, ch. 12, pp. 623-719.

[8] Borkar, T.Karnik, S.Narendra, J.Tschanz, A. Keshavarzi and V.De " Parameter Variations and impact on circuits and microarchitecture," in Proc, DAC, Jun,2003, pp.338-342.