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# Design of High Speed and Low Power Dadda Multiplier using Different Compressors

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ABSTRACT

Multipliers are vital components of any processor or computing machine. The performance of microcontrollers and digital signal processors are evaluated on the basis of number of multiplications performed in unit time. To increase speed and to reduce power the dadda multiplier used with different compressors. The use of compressors in the multipliers not only reduces the vertical critical path but also reduce the stage operation simultaneously. The speed of the dadda multiplier is improved by introducing different compressors instead of 4:2compressors. In this paper 4:3, 5:3, 6:3 and 7:3 compressors are used to reduce the stages of multiplication by reducing the number of half adders and full adders. This give chances for modular design where smaller block can be used to design a bigger one. Employing this technique in the computations algorithms will reduce the execution time, power.

## 1. INTRODUCTION

Now a day's multiplier is one of the most important blocks in any processor and arithmetic operations. Multiplication requires substantially more hardware resources and processing time than addition and subtraction. Since the multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. A number (multiplicand) is added to itself a number of times as specified by another number (multiplier) to form a result (product). But the implementation of multiplier takes huge hardware resources and the circuit operates at low speed. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the real time system [6]. Multiplier requires more hardware resources than the adder and subtractor. Improving the performance and reducing the power dissipation of the systems are the most important design challenges for Embedded and DSP applications.

The Dadda multiplier is a hardware multiplier design, invented by computer scientist Luigi Dadda in 1965. It is one type of parallel multiplier. It is slightly faster (for all operand sizes) and requires fewer gates (for all but the smallest operand sizes) than array multiplier Dadda multipliers have less expensive reduction phase. Compared to a Wallace tree, which requires ten full adders and half adders, the reduction phase of the Dadda multiplier requires only six [2]. The Dadda Multiplier requires less hardware than the Wallace. Compressors are primary component of the multiplier. Large delay was observed in partial products addition stage that increase the amount of power consumed. Using compressor adders, that add four, five, six or seven bits at a time, the number of full adders and half adders are reduced and hence the power consumed is less. Compressors are building blocks used for accumulating partial products during the multiplication process [3]. The basic idea in an n: 2compressor is that n operands can be reduced to two, by doing the addition while keeping the carries and sums separate.

## 2. LITERATURE REVIEW

In paper [5] improved version of the tree based multiplier architecture is called Wallace tree multiplier is proposed. It uses carry save addition algorithm to reduce the latency. This paper aims to further reducing the latency and

power consumption of the Wallace tree multiplier and it is accomplished by using 4:2 and 5:2 compressors. In the proposed architecture, partial product reduction is accomplished by the use of 4:2, 5:2 compressor structures and the final stage of addition is performed by a proposed carry select adder. Two full adders are replaced by a single 4:2 compressor and 5:2 compressors replace three full adders. The disadvantage is the usage of more hardware increase the power consumption. In paper, [1] the 5:2 compressor is to reduce the stages of dadda multiplier is used. The 5:2 compressor is implemented by series connection of three Full Adder (FA) blocks. It connect five the inputs and give the two outputs which is connected to the next block in that way the number of gate and the number of adders are reduced. So the power and speed is improved. The disadvantage in the second design is its delay is high compared to design.

In this paper, [8] the author presents 4:2 compressor using two different 8T full adder designs. The aim of this paper is to reduce the power consumption of 4:2 compressor without compromising the speed and performance. A multiplier is typically composed of three stages- Partial products generation stage, partial products addition stage, and the final addition stage. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing. The author first describes about the 4:2 compressors which consists of 5 inputs and 3 outputs. It is called compressors since it compress four partial products into two.

In this paper, [10] there are several multipliers available to increase the performance level in the design field. Row bypassing multiplier with adaptive hold logic is used to reduce the power and area. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, this architecture can be applied to a column- or row-bypassing multiplier. This architecture increased delay. To overcome an appropriate design of an approximate compressor, multipliers can be designed for DSP applications.

In this paper the partial product stages are reduced by using the 4:2 compressor. The 4:2 compressor is to reduce the stages of dadda multiplier. The 4:2 compressor is implemented by series connection of two Full Adder (FA) blocks. The arrays of partial products are generated in the first step and it is compressed into minimum level of stages by using the 4:2 and 3:2 compressor. The disadvantage of this method is it requires more transistor count.

## 3. SYSTEM DESIGN

### *3.1 Conventional Dadda Multiplier*

Dadda multipliers do as few reductions as possible. Because of this, dadda multipliers have a less expensive reduction phase, but the numbers may be a few bits longer, thus requiring slightly bigger adders. To achieve this, the structure of the second step is governed by slightly more complex rules than in the Wallace tree. As in the Wallace tree, a new layer is added if any weight is carried by three or more wires. The reduction rules for the Dadda tree, however, are as follows:

1. Take any three wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each three input wires
2. If there are two wires of the same weight left, and the current number of output wires with that weight is equal to 2 (modulo 3), input them into a half adder. Otherwise, pass them through to the next layer
3. If there is just one wire left, connect it to the next layer [4].

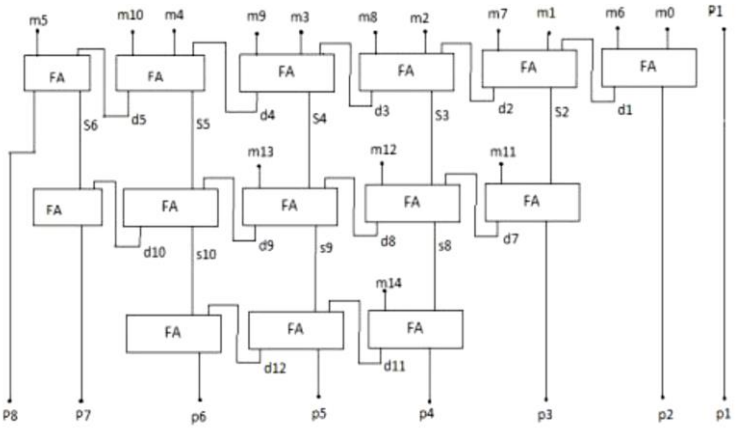


Fig: 1 4x4 Dadda multiplier

## 4. PROPOSED METHOD

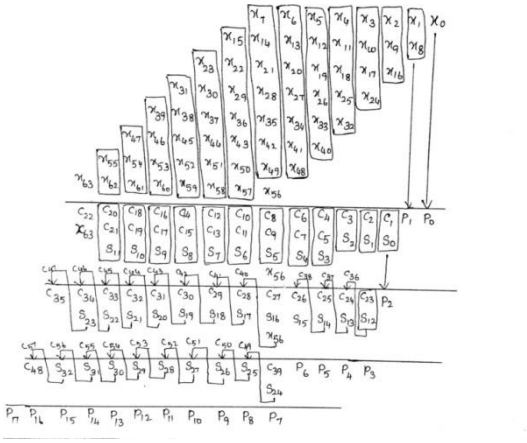

Fig: 2 8x8 dadda multiplier using compressor

Dadda Multiplier uses in the first part, the AND gates to generate all partial products. In first stage, two full adder, two half adder and nine compressors are used. In second stage, nine full adders and four half adders are used. In third stage, two half adders and eleven full adders are used. In fourth stage, ten half adders are used.

### *4.1 COMPRESSOR*

***Compressor [4:3]***

In a 4:3 compressor, if A, B, C and D are the inputs and Z2, Z1 and Z0 are outputs then Z2, Z1 and Z0 provides the count of the number of 1's at inputs A,B,C and D.

***Compressor [5:3]***

A combinational logic circuit of 5:3 compressor is a topology accepting five inputs and generating three outputs. The five input bits are summed up to produce the three bit output. The conventional design of 5:3 compressor is an enhanced version of 4:3 compressor and can have maximum value of 101 when all the three bits are 1.

***Compressor [6:3]***

In a 6:3 compressor, if A, B, C , D, E and G are the inputs and Z2, Z1 and Z0 are outputs then Z2, Z1 and Z0provides the count of the number of 1's at inputs A, B, C, D, E and G [9].

***Compressor [7:3]***

In a 7:3 compressor, if A, B, C , D, E, G and F are the inputs and Z2, Z1 and Z0 are outputs then Z2, Z1 and Z0provides the count of the number of 1's at inputs A, B, C, D,E, G and F.

## 5. SIMULATION RESULTS

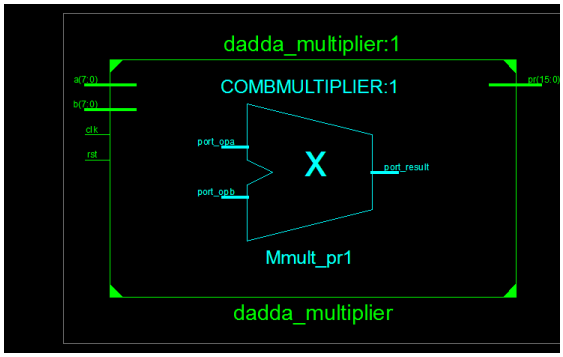


Fig:3 RTL schematic

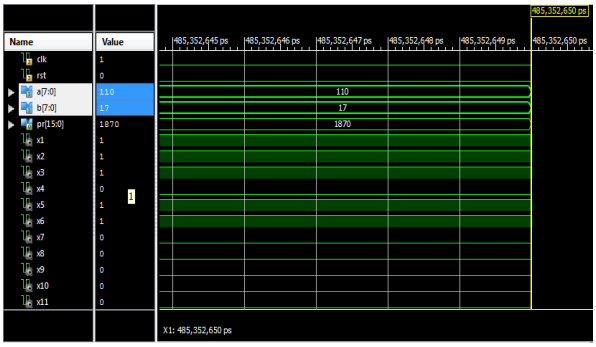


Fig:4 Output Waveform

Table 1. Experimental result of dadda multiplier using different compressors and comparison between delay, power and area

| Logic | Delay | Total power |
|---|---|---|
| Dadda multiplier using 4:2 compressor | 11.929ns | 325mw |
| Dadda multiplier using different compressors | 6.477ns | 322mw |

## 6. CONCLUSION

The implemented design in this work has been synthesized using Xilinx 14.5i. The simulated files are imported into the synthesized tool and corresponding values of delay and power are noted. The synthesized report contains area and delay value for Dadda multiplier different compressor. From these comparison results, it is clear that the delay calculation of our proposed method is reduced 45.70%, when compared to existing method. In Dadda multiplier using different compressor power consumption is also decreased. In future, this project can be extended to produce accurate results by implementing with more types of compressors such as 8:2, 9:2 and 15:2.

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