

Static Power Analysis of 4x4 Multipliers using Power Gating Technique

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ABSTRACT

In Today's VLSI design methodologies, low power consumption and high speed are essential factors. Since low power circuits are most important in designing microprocessors and system mechanism. Power minimization is one of the primary concerns methodologies because of two reasons one is the long battery operating life requirement of portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation. Since most VLSI systems include multipliers, power minimization in multipliers plays an important role. This can be achieved using Power gating technique. Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. Thus the power analysis of multipliers is made with and without the application of power gating technique and the efficient method is figured out.

Keywords: Delay calculation, Electric software, Multipliers, Power gating, Power minimization.

I. INTRODUCTION

Being a core part of arithmetic processing unit, multipliers are in extremely high demand on its speed and low power consumption. Multipliers play an important role in today's digital signal processing and various other applications. Thus, increasing the performance of the multipliers leads to the enhancement of the overall system performance. Analysis is done on the multipliers on the basis of physically compact high speed and low power consumption unit. Power Gating technique is discussed in chapter II followed by software used and types of multipliers in chapters III and IV. The result is obtained and concluded in chapters V and VI.

II. POWER GATING TECHNIQUE

Power gating has become one of the most widely used circuit design techniques for reducing leakage current. It's thought is very simple but its application to standard cell VLSI designs involves many careful considerations. The great complication of designing a power-gated circuit originates from the side effects of inserting current switches which have to be determined by a mishmash of extra circuitry and customized tools and methodologies. Topics include output isolation and data withholding current switch design and sizing and physical design issues such as power networks increases in area and wire length and power grid analysis. Standby leakage is in general smaller than active leakage. The device operating at room temperature substantially greater leakage power consumption compared to a few generations ago. Technology scaling calls for a reduction of the supply voltage to restrain power density. The sleep transistor can be turned off when the low- V_{th} logic block is still therefore resulting in a important reduction of sub-threshold leakage current.

III. SOFTWARE USED

The Tool used in for the analysis is **Electric VLSI design system**. The Electric VLSI Design System is an EDA tool written in the early 1980s by Steven M. Rubin. Electric is used to draw schematics and to do integrated circuit

layout. It can also handle hardware description languages such as VHDL and Verilog. The system has many analysis and synthesis tools, including Design rule checking, Simulation, Routing, Layout vs. Schematic, Logical Effort, and more. Electric is currently part of the GNU project and has been developed in Java and distributed as free and open-source software, subject to the requirements of the GNU General Public License (GPL), version 3 or any later.

IV. TYPES OF MULTIPLIER

A Multiplier is an electronic circuit used in digital electronics, such as computer, to multiply two binary numbers. It is built using binary adders. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of partial products, and then summing the partial products together. The types of multipliers taken in this paper are:

- (i) Array Multiplier
- (ii) Wallace Tree Multiplier
- (iii) Bough-Wooley Multiplier
- (iv) Vedic Multiplier

4.1. Array Multiplier

Array multiplier is a digital combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders and half adders. Array multiplier is well known for its regular structure.

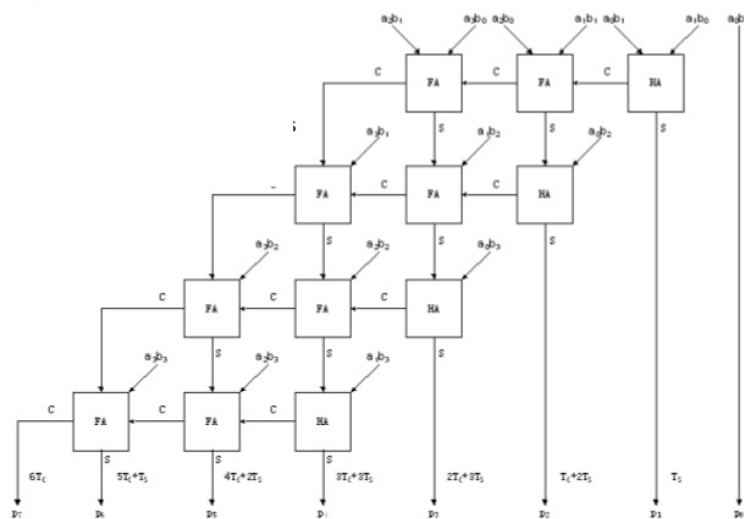


Fig.4.1 Block diagram of Array Multiplier

4.2. Wallace Tree Multiplier

The Wallace tree multiplier is considerably faster than a simple array multiplier because its height is logarithmic in word size, not linear. As a result, Wallace trees are often avoided by designers, while design complexity is a concern to them. The Wallace tree multiplier is a high speed multiplier.

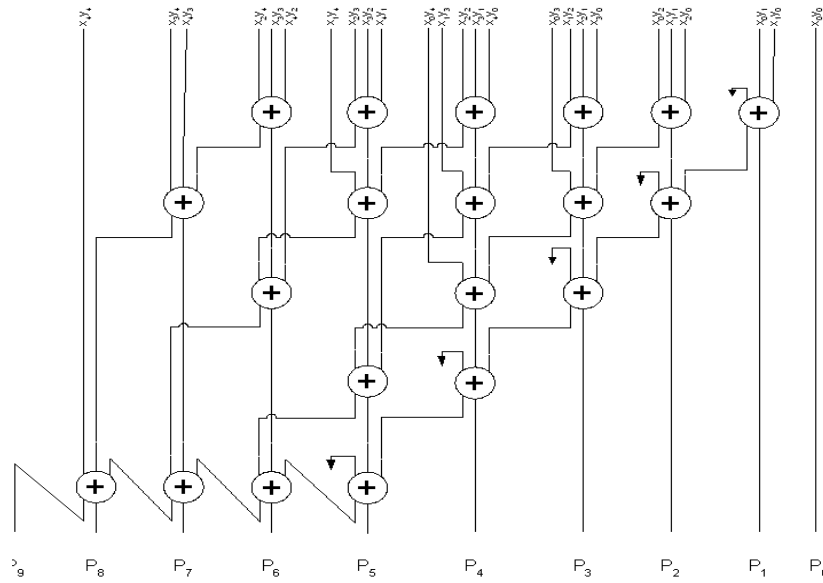


Fig.4.2 Block diagram of Wallace Tree Multiplier

4.3. Baugh Wooley Multiplier

It is used for signed numbers multiplication. Baugh Wooley technique was developed to design direct multipliers for two's complement numbers. When multiplying two's complement numbers directly, each of the partial products to be added is a signed number.

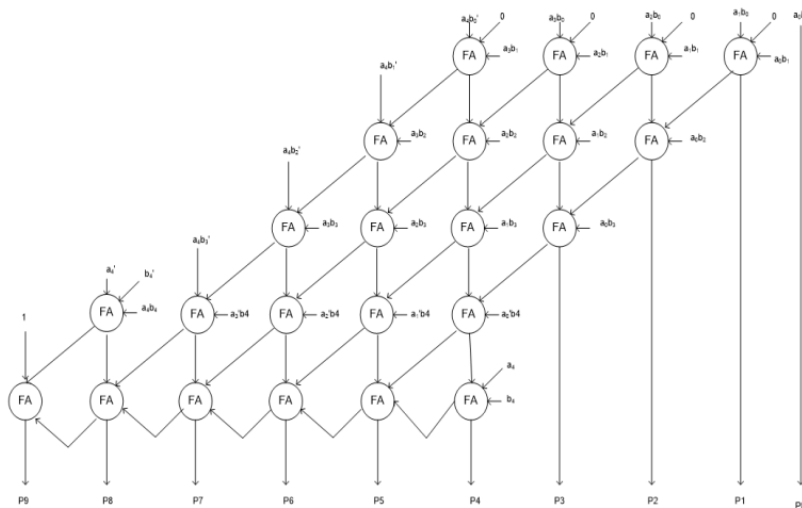


Fig.4.3 Block diagram of Baugh Wooley Multiplier

4.4. Vedic Multiplier

The multiplier is based on an algorithm URDHVA TIRYAKBHYAM of ancient Indian Vedic Mathematics. URDHVA TIRYAKBHYAM SUTRA is a general multiplication formula applicable to all cases of multiplication. It literally means “vertically and crosswise”.

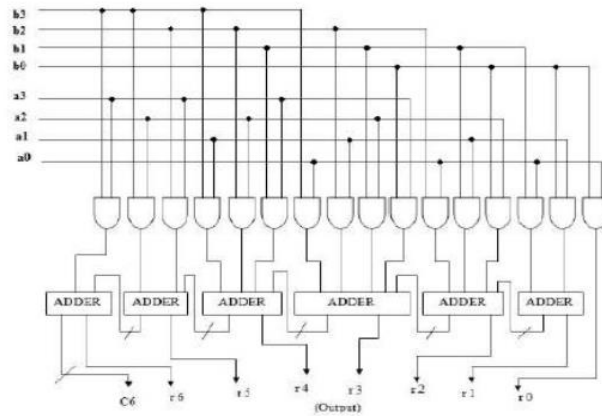


Fig.4.4 Block diagram of Vedic Multiplier

V. RESULTS AND DISCUSSION

The comparison on different types of multipliers is done and the result obtained as:

5.1. Comparison on Power consumption

Parameter	Array Multiplier	Wallace Tree Multiplier	Baugh Wooley Multiplier	Vedic Multiplier
Power consumption without Power Gating	2.308uW	1.364uW	1.774uW	1.026uW
Power consumption with Power Gating	1.51uW	0.766uW	1.463uW	0.984uW

Fig.5.1 (a) Power comparison table

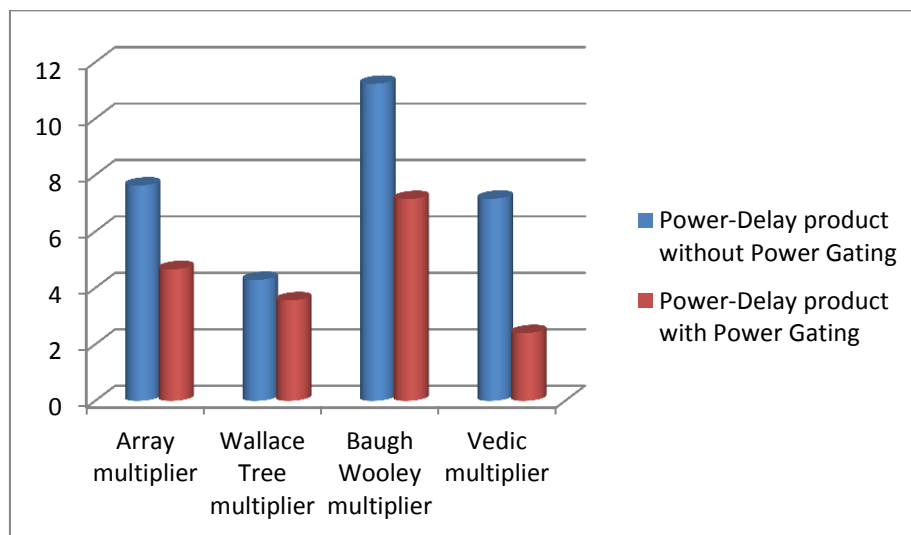


Fig.5.1 (b) Power comparison chart

5.2. Comparison on Delay

Parameter	Array Multiplier	Wallace Tree Multiplier	Baugh Wooley Multiplier	Vedic Multiplier
Delay without Power Gating	3.306s	4.175s	6.334s	5.250s
Delay with Power Gating	3.090s	3.620s	4.887s	3.134s

Fig.5.2 (a) Delay comparison table

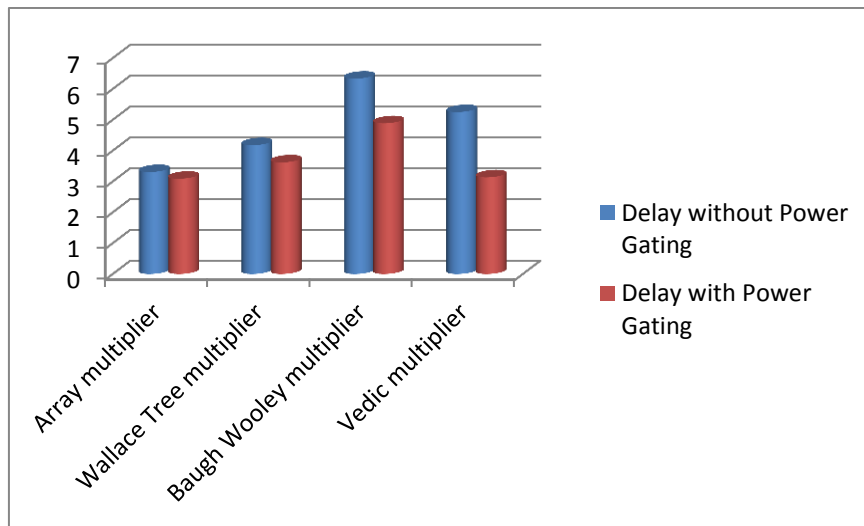


Fig.5.2 (b) Delay comparison chart

5.3. Comparison on Power-Delay product

Parameter	Array Multiplier	Wallace Tree Multiplier	Baugh Wooley Multiplier	Vedic Multiplier
Power-Delay product without Power Gating	7.630uWs	4.283uWs	11.236uWs	7.161uWs
Power-Delay product with Power Gating	4.665uWs	3.562uWs	7.149uWs	2.400uWs

Fig.5.3 (a) Power-delay product comparison table

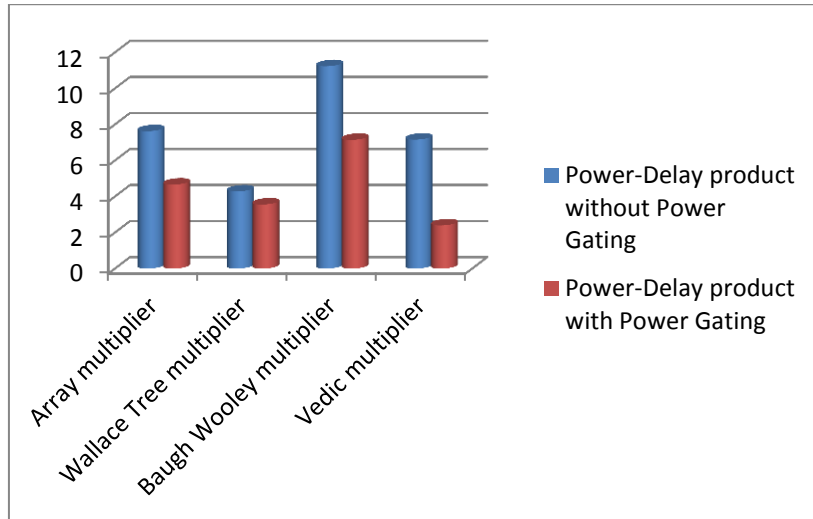


Fig.5.3 (b) Power-delay product comparison chart

VI. CONCLUSION

This research has achieved good results and demonstrated the efficiency of high level optimization techniques. Power gating technique proves to be good in reduction of power in case of multipliers. Hence it's been able to develop arithmetic algorithm and architectural level optimization techniques for low power multiplier design. From the analysis, it can be concluded that the average power consumption of the four multipliers with power gating is 1.1807uW and therefore the power consumption has reduced by 72.97% by the usage of power gating technique. Similarly, the average delay of the four multipliers with power gating is obtained as 3.682s and the parameter is reduced by 77.26% and the average power-delay product of the four multipliers is 4.44uWs and it is reduced by 58.64% by the usage of power gating.

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